32nd International Electronics Manufacturing Technology Symposium

Advanced Packaging Materials Symposium

October 3-5, 2007 San Jose/Silicon Valley, CA USA

Co-located for the first time!
One registration admits you to all sessions and events.

Summary of the IEMT/APM Symposium (details inside)

SESSIONS

Thursday, October 4
- Stacked Die and Die-Attach Film
- Manufacturing Technology
- Materials for Electronics Packaging
- Imaging, Medical, Embedded Technology
- Materials in Packaging Applications
- Posters Session
- Exhibits, Reception, Evening LEOS Meeting

Friday, October 5
- Materials for Interconnects
- Lead-free Soldering and Bonding
- Packaging for MEMS, 3D, WLP
- Nanotechnology
- Design for Environment

PROFESSIONAL DEVELOPMENT COURSES

Wednesday, October 3

Four Morning PDCs:
- **Nanotechnology Applications in Packaging,** Florin Ciontu, NanoSPRINT
- **Implementing Flip Chip and WLP Technology,** Peter Elenius, E&G Technology Partners
- **Advanced Packaging Technology Solutions for Today's Leading Edge Microelectronics**, Charles B. Woychik, GE Global Research
- **Achieving High Reliability for Lead-Free Solder Joints - Materials Considerations,** Dr. Ning-Cheng Lee, Indium Corporation of America

Three Afternoon PDCs:
- **Polymers & nano-Composites for Electronic and Photonic Packaging: Recent Advances in Materials and Processes,** Prof. C.P. Wong, Georgia Institute of Technology
- **3-Dimensional Semiconductor Packaging & Integration,** Charles E. Bauer, Ph.D., and Herbert J. Neuhaus, Ph.D., TechLead Corporation
- **Failure Modes & Analysis of Flip Chip Assemblies**, Prof. Daniel Baldwin, Georgia Institute of Technology

GALA RECEPTION

Thursday, October 4 Western-themed BBQ and Reception, featuring the Silicon Cowboys rock group (songs from the '60's, '70's and '80's), featuring Tom Tarter, 2005 IEMT General Chair

EXHIBITS

Thursday, October 4	11 AM – 6 PM
and Friday, October 5	10 AM – 3 PM

Register On-line: www.cpmt.org/iemt or /apm Discount through Sept. 17, 2007

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Exhibitors:

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To request an invitation letter to accompany your USA visa application, please email Paul Wesling, p.wesling@ieee.org

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Dr. G.Q. Zhang	NXP Semiconductors, Netherlands

Wednesday, October 3, 2007

HALF-DAY **MORNING PROFESSIONAL DEVELOPMENT COURSES**

(Choose from Four) AFTERNOON Courses: Page 5

PDCs Chair: Dr. Charles E. Bauer, TechLead Corporation

8:00 AM: **Registration**

8:30 - Noon: Nanotechnology Applications in Packaging

Florin Ciontu, France .... NanoSPRINT

This course provides a strategic-level update on areas of nanotechnology research likely to impact semiconductor packaging. The course first introduces fundamental nanotechnology concepts such as carbon nanotubes and nanoparticles and then focuses on potential solutions to three industry issues facing advanced semiconductor packaging: heat-dissipation, low-temperature assembly and IC/package stress.

For each solution, the instructor reviews emerging technology options in terms of performance, relevant physical mechanisms, advantages, and the activities of the leading research groups. Where appropriate, the discussion includes profiles of existing nanotechnology start-ups and their approaches.

The tutorial ends with a comparative discussion of technology readiness levels and patenting activity for the solutions previously presented. A detailed analysis of the most active players and a discussion of the most appropriate strategies for getting involved in this area completes the tutorial. Outline:

Introduction

- Opportunities in nanotechnology
  - Review of critical scales and associated phenomena
  - Paradigm shifts introduced by nanotechnology
- Fundamental concepts: carbon nanotubes, nanoparticles, nanowires, etc.

Heat-Dissipation solutions

- Thermal Interface Materials
  - Vertically-grown carbon nanotubes
  - Nanotube and nanoparticle composites
- Microchannel coolers
  - Integrated carbon nanotubes

Low-temperature assembly

- Low-reflow-point solders
  - Nanoparticle-based solders
- Conductive Adhesives
  - Wet-adhesives using metal nanopowders
  - Wet-adhesives reinforced by carbon nanotubes
  - Dry-adhesives using carbon nanotubes

Thermo-mechanical fatigue and IC/package stress

- Reinforced Solders
- Nanotube-reinforced joints
- Nanoparticle reinforced solders

Conclusion

- Comparative analysis of the technology readiness levels of different solutions
- Analysis of the most active players
- Discussion of partnerships, strategies and technology transfer opportunities

Intended Audience

- Packaging Engineers
- R&D Managers
- Technology Transfer Managers
- Financial Analysts

Florin Ciontu, President of NanoSPRINT (a leading provider of technology intelligence for nanotechnology professionals), pursued research at TIMA Labs in Grenoble, France where he initiated and coordinated a program focusing on nanotechnology. Prior to TIMA, Florin developed algorithms for implementing on-chip fault tolerance to radiation effects at iRoC Technologies. Florin holds a CS Engineer Diploma from "Polytechnica" University of Bucharest and participates in a variety of programs focusing on contributions of technology to sustainable socio-economic development.

NanoSPRINT spun out of TIMA Labs, with Florin as one of the founders, to develop proprietary tools facilitating extensive analysis of specific areas in terms of technological developments, players involved in the field and funding sources. For the past three years, NanoSPRINT has organized NanoTRANSFER – the Nanotechnology Transfer Executive Summit in Europe.

8:30 – Noon: Implementing Flip Chip and WLP Technology

Peter Elenius...................................... E&G Technology Partners

This course focuses on the implementation of flip chip (FC) and wafer level packaging (WLP) bumping technologies. The course material covers the selection of the appropriate technology, the processes used and challenges encountered in the deployment of flip chip and wafer level package manufacturing.

Course Outline

- What drives flip chip (FC) and wafer level package (WLP) adoption.
- Common FC and WLP bump structures including a review of the Intel Cu-Post technology.
- Overview of FC and WLP bumping processes, materials and equipment.
- Available solder alloys, including benefits, drawbacks and how to choose.
- Processing issues that impact yield.
- Reliability failure mechanisms, including thermal cycle, electromigration and diffusion.
- Failure analysis techniques to identify processing issues and reliability failures.

Intended Audience

Target audience includes individuals and companies currently using or considering the use and/or deployment of FC or WLP technology. Especially beneficial to those outsourcing their production, the course provides a fundamental understanding of the technology options available, the processes employed and relevant issues that arise.

About the Instructor:

A founder and managing partner at E&G Technology Partners (a firm specializing in technology commercialization and business development), Peter Elenius's experience with Flip Chip and WLP technologies spans more than 25 years. He helped establish Flip Chip Technologies (FCT) where he served as VP of Technology and CTO. Prior to FCT he worked at Kulicke & Soffa and IBM in flip chip related technologies. Recognized world wide as an expert in flip chip and wafer-level packaging technologies, Peter speaks at numerous conferences, publishes a wide range of papers and holds ten patents in the field of advanced packaging. Peter earned an MS degree in Manufacturing Systems and a BS in Mechanical Engineering from the University of Wisconsin – Madison before entering the industry at IBM.

Additional Morning PDCs =====>

8:30 – Noon: Advanced Packaging Technology Solutions for Today's Leading Edge Microelectronics

Charles G. Woychik, Ph.D .... GE Global Research

This course explores advanced packaging solutions for next generation microelectronics by looking at three key applications driving packaging and interconnection developments. The instructor reviews technology trends, market segments, application requirements, packaging approaches and electronic material developments.

While semiconductor device trends in I/O count, power, bias voltage, and clock rate define advanced packaging needs; three key electronics market segments – Cost-Performance Electronics, Portable Electronics and Automotive Electronics – provide the impetus directing packaging technology developments. The course analyzes the unique needs and characteristics of these market segments and the latest packaging advancements each segment drives. After analyzing wire bond vs flip chip, area array packages vs leaded carriers, and BGA vs Chip Scale and Flip Chip, the instructor examines trends in high density interconnect structures, optical interconnections, integrated passives and 3-D electronics. Additional material addresses the special packaging needs for MEMS devices, the effect of changing environmental requirements such as lead free on packages, assembly and materials as well as critical materials development needs for thermal interface materials (TIMs), underfill materials, molding and protective coating materials. Specific examples of advanced packaging developments at GE Global Research illustrate the opportunities and impact of advanced packaging technologies in the industry.

Course Outline

- Objective
- Semiconductor Trends
- Advanced Pkgng Trends
- Multichip Technologies
- Flip Chip and Chip Scale
- Automotive Electronics
- Integral Passives
- 3-D Electronics
- LEDs and OLEDs
- Underfill Developments
- Thermal Interface Developments
- Evolving Microelectronics Arena
- Key Electronics Market Segments
- Cost-Performance Electronics
  - Portable Electronics
  - Electrical/Optical Interconnects
  - Interconnection Structures
  - Optical Interconnects
  - MEMS Packaging
- Electronic Materials Opportunities

Intended Audience:

This tutorial targets new entrants to the packaging and interconnection field; suppliers of materials; components and equipment to the microelectronics fabrication and assembly industry; and users of electronics. It provides a strong historical background on the microelectronics industry; and provides the attendee a glimpse of the future directions expected in the packaging and interconnection of semiconductors and optical components

Course Instructor:

Charles G. Woychik received his Ph.D. in Materials Science and Engineering from Carnegie-Mellon University in 1984. He joined IBM in Endicott, NY working in the area of soldering and materials selection for electronics packaging. He held both technical and managerial positions at IBM during his 18 year career there. In 2002, he joined Advanced Semiconductor Engineering (ASE) Inc. in the position of Director of Engineering and Technical Programs. In 2004 he moved to Plexus Corporation where he lead the Microelectronics organization until joining GE Global Research, where he currently develops electronic packages for healthcare diagnostics applications, in 2005.

8:30 – Noon: Achieving High Reliability for Lead-Free Solder Joints - Materials Considerations

Dr. Ning-Cheng Lee .... Indium Corp.

This course covers in detail the materials considerations required for achieving high reliability for lead-free solder joints. Reliability discussion includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions, and how those IMCs affect the reliability. Failure modes, thermal cycling reliability, and fragility of solder joints as a function of materials combination, thermal history, and stress history as well as the impact of novel alloys with reduced fragility provide insight into the details of materials impact on Pb free solder joints. Electromigration, corrosion, and tin whiskers as failure mechanisms further demonstrate the importance of materials in electronics assemblies. Furthermore, the course reviews the reliability behavior of through-hole solder joints and provides recommendations, particularly for thick boards. The emphasis of this course focuses on the understanding how various factors contribute to various failure modes, and how to select proper solder alloys and surface finishes to achieve high reliability. The instructor also includes descriptions of desirable future alloys and fluxes to meet the ongoing challenges of miniaturization.

- Prevailing Materials: Solder Alloys; Surface Finishes
- Mechanical Properties: Shear & Pull Strength; Creep
- Intermetallic Compounds
  - Interaction of Cu and Ni
  - Effect of Ni in Cu Pad
  - Effect of Cu Content in SAC
  - Effect of Alloy Additives
- Failure Modes
  - Grain Boundary Sliding & Cavitation
  - Grain Orientation
  - Mixed Alloys
  - Grain Coarsening
  - Lead Contamination
  - Interfacial Voiding
- Thermal Cycle Reliability
  - Thermal Cycle Tests
  - Effect of Reflow Temp
  - PCB Surface Finish Cu vs Ni
  - Reworked SMT Joints
- Reliability of Through-Hole Joints
- Fragility/effects of Lead-Free Solder Joints; of Component Finish; of IMC Thickness; of Isothermal/Thermal Aging; of Intermetallic Morphology; Novel Alloys with Reduced Fragility
- Electromigration: Influence of Temperature/Current on Resistance, IMC Thickness, Mechanical Properties
- Corrosion with SAC405; with PWB Finishes
- Tin Whiskers

Intended Audience:

This course is targeted to those wishing to understand high reliability lead-free solder joints and how to achieve them.

Course Instructor:

Dr. Ning-Cheng Lee, Vice President of Technology for Indium Corporation of America since 1986, previously worked at Wright Patterson Air Force Base Materials Laboratory, Morton Chemical, and SCM. With more than 22 years of experience in the development of fluxes and solder pastes for the SMT industry, he received his PhD in polymer science from Univ of Akron and a BS in chemistry from National Taiwan Univ. The author of "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies" and co-author of "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials," Ning-Cheng also authored book chapters for several lead-free soldering books. He holds the honor of 2002 SMTA Member of Distinction, received 2003 Lead-Free Cooperation Award from Soldertec, and received the 2006 Exceptional Technical Achievement Award from the IEEE's CPMT Society. He serves on the Board of Directors for the SMTA, and previously served on the Board for CPMT.

Wednesday, October 3, 2007

HALF-DAY **AFTERNOON** PROFESSIONAL DEVELOPMENT COURSES

(Choose from Three)

1:00 – 4:30: Polymers & Nano-Composites for Electronic and Photonic Packaging: Recent Advances in Materials and Processes

Prof. C.P. Wong .... Georgia Institute of Technology

Polymers are widely used in electronics packaging as adhesives, encapsulants, insulators, dielectrics, molding compounds and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high performance novel No Flow Underfills, Reworkable Underfills for Ball Grid Array (BGA), Chip Scale Packaging (CSP), System on a Package (SOP), Direct Chip Attach (DCA), Flip-Chip (FC), Paper-thin ICs and 3D Packaging, Conductive Adhesives (both ICA and ACA), Embedded Passives (high-k polymer composites), nano particles and nano-functional materials. It is imperative that materials suppliers, formulators and their users have a thorough understanding of polymeric materials and the recent advances in nano materials and their importance in advancements within the electronics packaging and interconnect technologies.

Course Outline:

- Overview of semiconductor packaging technology
- The next generation of electronics packaging
- Novel no flow and reworkable underfills for flip-chip applications
- Fundamentals and recent advances in conductive adhesives and nano lead-free Alloys for lead-free Interconnects
- Conductive adhesives and nano-lead-free alloys for lead-free interconnects: fundamentals and recent advances
- Low-cost high-performance embedded passives materials and processes
- Recent advances in nano particles and nano-functional Materials

WHO SHOULD ATTEND:

Engineers, scientists and managers involved in the design, process and manufacturing of IC electronic components and hybrid packaging; electronic materials suppliers involved in materials manufacturing and research & development.

About the Instructor:

Dr. C.P. Wong is a Regents' Professor and the Charles Smithgall Institute Endowed Chair (one of the two Institute endowed chairs at Georgia Tech). His research interests lie in the area of polymeric materials (organic and inorganic), and nano functionalized materials, in particular, low-cost, high-performance materials and manufacturing processes. Prior in joining Georgia Tech in 1996, he was with AT&T Bell Laboratories for 19 years and was elected as an AT&T Bell Labs Fellow in 1992. He holds over 45 U.S. patents, numerous international patents, and has published over 500 technical papers and 450 presentations in packaging related areas. Dr. Wong received the B.S. degree in chemistry from Purdue University, the Ph.D. degree in chemistry from Penn State University, and was a Postdoctoral Fellow at Stanford University. He has received many Awards from the IEEE, IMAPS, AT&T Bell Labs, and Georgia Tech. The IEEE CPMT Society Sustained Technical contributions award in 1995, the IEEE EBA Award in Continuing Education in 2001, the CPMT Exceptional Contributions Award in 2002, the Georgia Tech Distinguished Professor Award in 2004, named holder of the Charles Smithgall Institute Chair in 2005 and the IEEE Components, Packaging and Manufacturing Technology award in 2006. He serves on six Editorial Boards of the IEEE Trans. on Components and Packaging Technologies, International Opto-electronics, Journal of Adhesion Science & Technology, the Journal of Nano-composites, Chip Scale Review and the John-Wiley Encyclopedia on Smart Materials. He is a fellow of the IEEE and is a member of the National Academy of Engineering of the USA.

1:00 – 4:30: 3-Dimensional Semiconductor Packaging and Integration

Charles E. Bauer, Ph.D., and Herbert J. Neuhaus, Ph.D., ... TechLead Corporation

The latest trend in miniaturization of electronics systems, 3D packaging of both active and passive devices, opens a new world of performance and integration to system designers. This course covers both the fundamental and advanced technologies in use today to produce both stacked chip packages as well as stackable packages for implementation of highly integrated mobile electronic products. These include the challenges of die thinning, thin die attach, multi-level wire bonding, mixed technology die attachment and bonding, flip chip and TAB. Substrate selection for various 3D packaging techniques including silicon tiles, flex circuit origami and specialty interposers concludes the chip-stacking section of the course. Several examples of specific 3D package structures demonstrate both the power and limitations of these approaches.

Further considerations for 3D electronics include stackable packages based on flex and rigid substrate approaches, integrated system-in-package (SiP) techniques and multilayer, embedded passive technologies. The course concludes with a review of the drivers behind 3D packaging and presentation of multiple examples of 3D packages in actual usage today.

Course Outline:

- 3D Package Trends
- 3D Package Applications
- Drivers for 3D Packaging
- Stacked Packages
  - Package on Package
  - Origami
  - Edge Stacked Modules
- Die Stacking
  - Wire Bond
  - Mixed Technology
  - Edge Redistribution
  - Through Silicon Vias
- 3D Integration (SiP)
- Issues in 3D Integration
- Intellectual Property Landscape for 3D Packaging

Instructors:

Charles E. Bauer, Ph.D. serves as Senior Managing Director of TechLead Corporation, a technology management company specializing in the electronics packaging, interconnection and assembly industry. Dr. Bauer focuses in the areas of strategic technology planning, market analysis and business development, primarily in the international arena. With more than 20 years experience spanning the range from printed circuit board and hybrid fabrication through complex IC metallization, multilayer packaging, multichip modules (MCMs) and flat panel display packaging and assembly, he brings tremendous breadth and depth to his work. Dr. Bauer lectures throughout the world on technology, business and market topics as well as serving on several corporate boards and

international corporate, government and educational institution advisory councils.

Chuck served ISHM as President of the NW Chapter, Technical Chair of the ISHM National Symposium in Seattle, National Technical Vice President of the Society and President of the Rocky Mountain Chapter. He founded the ISHM/IMAPS Advanced Technology Workshop program and served as General or Technical chair for several ATWs between 1990 and 1998. Dr. Bauer also served on the Board of Directors of the SMTA from 1997 through 2001 when elected President of IMAPS for 2001-2002. He now serves as Chair of the SMTA International Development Committee and remains active internationally with the SMTA, IEEE, IMAPS, JIEP and ASM.

Herbert J. Neuhaus, Ph.D. serves as Director of Operations of TechLead Corporation, where he supports clients throughout the world in the areas of intellectual property management and valuation as well as technical cost modeling and develops strategic planning tools. Active since 1980 in the development and characterization of electronic materials and associated manufacturing processes for a wide variety of applications including flip-chip for RFIDs and Smart Cards, LED assembly, chip interconnect and passivation, multichip modules, printed wiring boards, and flat panel displays, Dr. Neuhaus synthesized a unique perspective on electronics packaging, interconnection and assembly industry.

Dr. Neuhaus received his Ph.D. degree in Physics from the Massachusetts Institute of Technology and holds the distinction of Fellow of the Society of the International Microelectronics and Packaging Society (IMAPS). He currently chairs the materials subcommittee of the IMAPS National Technical Committee and serves on the Board of Directors of Vyta Corp.

1:00 – 4:30: Failure Modes and Analysis of Flip Chip Assemblies

Prof. Daniel Baldwin................. Georgia Institute of Technology

Several material and process technology advances recently emerged for flip chip assembly processing such as fast-flow snap-cure underfills, no-flow underfills, emerging wafer scale underfills and associated innovative process technology. While a large number of technical publications help with understanding basic process requirements, understanding of failure modes and reliability standards remains essential for these technologies to gain traction in the industry. This course presents reliability test procedures, frequently encountered process defects and common failure modes that occur in flip chip packages and board level flip chip assemblies. The course focuses on accelerated reliability tests, process defect identification and resolution, failure mechanisms and the associated analysis tools needed to identify them such as FTIR, XRF, transmission X-ray analysis, acoustic microscopy and scanning electron microscopy. Descriptions of numerous process defects and failure modes presented along with extensive visual aids provide a more intuitive understanding of the defects and failure modes associated with these advanced assemblies. The course also discusses artifacts leading to process defects and how they contribute to premature failure.

Topics:

- Reliability Tests
- Destructive and Non-Destructive Failure Analysis and Equipment
- Process Defects and Effects on Failure and Reliability
- Reliability Modeling
- Failure Modes and Reliability Implications
- Delamination and Void Growth
- Solder Migration
- Solder Extrusion
- Die Cracking – Center
- Die Cracking – Edge
- Underfill Cracking – Fillets
- Underfill Cracking - Bulk
- Solder Fatigue
- UBM Pad Lift
- Solder Creep Fracture
- Gold Embrittlement
- Interconnect, Substrate, and Chip Design Factors
- In Situ Stress Analysis of Flip Chip Assemblies

Who Should Attend

Target audience includes individuals and companies associated with electronics packaging, particularly package reliability, failure analysis, and assembly process control/defects. The course should prove especially valuable to:

- Managers. Knowledge gained through this course will allow managers to make informed decisions about the technical feasibility, implementation factors, performance benefits, reliability, and risks of implementing flip chip technology.
- Engineers. Manufacturing, quality, design, and packaging engineers in integrated circuit, equipment, materials, and system design who must solve process defect and packaging problems. Knowledge gained through this course will allow engineers and technologists to make informed decisions about the technical feasibility, implementation factors, performance benefits, reliability, and risks of implementing flip chip technology.

Instructor:

Dr. Daniel Baldwin was a Member of the Technical Staff at Bell Laboratories before coming to Georgia Tech in 1995. He has a diverse research background, which provides a broad range of experience in manufacturing fundamentals and the engineering sciences. His early research was in assembly processes and assembly system design; he developed methodologies and software tools to aid in the design of assembly systems used to produce complex mechanical assemblies, such as automotive transmissions and engines. His research interests then expanded into the field of polymer processing, focusing on the system level design and development of new and innovative process technologies for the production of novel microcellular foam materials. Dr. Baldwin's research expanded during his tenure at Bell Laboratories to work in electronics manufacturing, assembly, and packaging.

Dr. Baldwin's research focus includes low-cost manufacturing of next-generation electronic assemblies. Competitiveness in the global electronics industry demands that the next generation of electronic assemblies realize a ten-fold cost reduction over current practice, while increasing performance and functionality and decreasing size and weight. This research addresses these demands through the development of innovative materials and process technologies.

He is active on smart tooling for the assembly of thin flexible systems. Here, emerging electronic assemblies demand lower cost, lighter weight, miniaturized packages mounted on thin, flexible circuit boards or flex circuits. This research seeks to develop such smart tooling for high-speed surface mount and high-volume packaging processes. He is also developing microelectromechanical systems (MEMS) and MEMS carriers for low-cost manufacturing.

Dr. Baldwin's research is sponsored by Siemens, the Defense Advanced Research Projects Agency, the National Science Foundation, Motorola, Chrysler, Cookson Electronics, Alpha Metals, Northrop Grumman, Loctite, and Georgia Tech.

REGISTER ON-LINE TODAY!

ADVANCE PROGRAM: Joint APM/IEMT Symposium

Thursday, October 4, Morning

8:00 AM **IEMT Symposium Opening and Welcome**
Dr. Srinivas Rao, Flextronics ....General Chair
Dr. KRS Murthy ....Program Chair

8:00 AM **APM Symposium Opening and Welcome**
Dr. Dongkai Shangguan, Flextronics............General Chair
Dr. Paul Wang, Microsoft Corp....................Program Chair

SESSION 1: 8:10 AM – 11:50 AM

IEMT: Manufacturing and Test Technology

Session Co-Chairs: Dr. Luu Nguyen, NSC; Frank Juskey, TQS

Complex Low Volume Electronics Simulation Tool to Improve Yield and Reliability
Diana M. Segura Velandia, Paul P. Conway, Andrew A. West, David Whalley, Antony Wilson, and Lina Huertas .... Loughborough University

What's Next after Process Characterization
Teh Eng Hooi, Cheah Fook Nyen, and Lee Wei Tsun .... ON Semiconductor

Effect of Abandon Time on Print Quality and Rheological Characteristics for Lead-Free Solder Pastes used for Flip-Chip Assembly
A.E. Marks, S. Mallik, and N.N. Ekere ....University of Greenwich at Medway, UK
R. Durairaj ....University Tuanku Abdul Rahman (UTAR)

Numerical and Experimental Study of Underfill Flow during Underfill Encapsulation of Flip-Chips
Sung-won Moon, Shripad Gokhale, Chun Keang Ooi, Jinlin Wang, and Zhihua Li .... Intel Corporation

Overmolded FC-SiP for Miniaturized Devices
Erik Jung, Matthias Koch, Karl-Friedrich Becker, Volker Bader, Rolf Aschenbrenner, and Herbert Reichl .... Fraunhofer IZM

Methods to Resolve Heel Stress for Ultra Thin QFN Small Package
Siew Han Looe, Soon Wei Wang, and Azhar Aripin .... ON Semiconductor

Test Base Analysis – Inferences from a Disposition Tree
Jia Keat Lee, Somnuk Amnuaisuk, and Chin Kuan Ho .... Multimedia University
Lee Hong Yong and Siew Beng Thum .... Intel

SESSION 2: 8:10 AM – 11:50 AM

APM: Materials for Electronics Packaging

Session Co-Chairs: Dr. Ning-Cheng Lee, Indium; Prof. Jinny Rhee, SJSU

Overmolded Flip Chip Packaging Solution for Large Die FPGA with 65nm Low-k Dielectrics
Laurene Yip and Raghunandan Chaware .... Xilinx

Fluxless Bonding of Silicon Chips to Ceramic Packages Using Electroplated Au/Sn/Au Structure
Pin J. Wang, Jong S. Kim, Chin C. Lee .... UC Irvine

Modeling Non-Coplanarity Effects on Thermal Performance of Computer Chips
Ninad Bhave, Nicole Okamoto San Jose State University

Effect of Product Design and Materials on Large Leadless Package Reliability
Jatinder Kumar, Won Yun Sung, and Shutesh Krishnan .... ON Semiconductor

Designer Heat Spreading Materials and Composites
Allen Amaro, Dr. K.R.S. Murthy .... Ultimate-Results.net

Performance-Cost Optimization of a Diamond Heat Spreader
Anita Rogacs .... Stanford University
Jinny Rhee .... San Jose State University

SESSION 3: 8:10 AM – 11:50 AM

IEMT: Stacked Die and Die-Attach Film

Session Co-Chair: Dr. Annette Teng, CORWIL Technology

Dicing Die Attach Film for 3D Stacked Die QFN Packages
Shahrum Abdullah .... Universiti Kebangsaan Malaysia

3D Electrical Interconnection Using Extrusion-Dispensed Conductive Adhesives
Lawrence D. Andrews, Terrence C. Caskey, and Simon J. S. McElrea .... Vertical Circuits, Inc.

Advances in Die Attach Films
Carlos Martinez ..... Lintec Advanced Technologies (USA)
Annette Teng, Ph.D. .... CORWIL Technology

Wire Bond Challenges of Stacked Dice Devices
Charles J. Vath, III, N. Srikanth, J. Premkumar, M. Sivakumar, and M. Kumar ... ASM Technology Singapore

Hygro-Thermal Finite Element Analysis of Green Stacked Die Package
Z.K. Hua, C.Y. Li, and J.H. Zhang .... Shanghai University
Y.X. Luo,L.Q. Cao .... Intel Technology Dev't (Shanghai)

Working Temperature Characterizations for Die Attach Films in Stacked-Die Process
Tsung-Yueh Tsai, Hsiao-Chuan Chang, Wei-Chung Li, Chi-Ping Teng, and Yi-Shao Lai .... Advanced Semiconductor Engineering, Inc.

Evaluation of Thermal Characteristics and Thermo-mechanical Reliability of Stacked-Die Packages under Coupled-Power and Thermal-Cycling Test Conditions
Tong Hong Wang, Chang-Chi Lee, Yi-Shao Lai, and Ching-Chun Wang .... Advanced Semiconductor Engineering

Exhibits Open: 11 AM – 6 PM

Thursday, October 4, Afternoon

SESSION 4: 1:30 PM – 4:45 PM

IEMT: Imaging, Medical, Embedded Technology

Session Co-Chairs: Dr. Brent K. Whitlock, Carr & Ferrell LLP, Jan Vardaman, TechSearch International

Compact Soft X-ray Lasers for Imaging, Material Processing, and Characterization at the Nanoscale
J.J. Rocca, M.C. MarconI, C.S. Menoni, P.W. Wachulak, B. Luther, F. Brizuela, C. Brewer, Y. Wang, D. Alessi, M. Berrill, D. Martz, S. Heinbuch, M. Grisham .... Colorado State University
W. Chao, E. H. Anderson, and D. T. Attwood .... Lawrence Berkeley National Laboratory

Trends in Microelectronic Assembly for Implantable Medical Devices
Robert Erich .... Medtronic Microelectronics Center

Medical Device Wafer Singulation
Annette Teng, Finn Wilhelmsen ...... CORWIL Technology

Embedded Components in IC Packages: New Applications and Trends
E. Jan Vardaman, Karen Carpenter .... TechSearch Int'l

Understanding the Cost Effectiveness of Embedded Technology
Chet A. Palesko, Alan C. Palesko ..... SavanSys Solutions

Embedded Capacitor Technology- A Real World Example
Norman Smith, Jim Knighten .... Teradata
Jun Fan .... UMR
John Andresakis .... Oak-Mitsui Technologies
Yoshi Fukawa .... TechDream
Mark Harvey .... Sanmina-SCI

——— SESSION 5: 1:30 PM –4:45 PM———

APM: Materials in Packaging Applications

Session Co-Chairs: Daniel Lu, Intel, Erik Jung, Fraunhofer IZM

iNEMI's Gap Analysis Based on the 2007 Electronics Roadmap
Alan Rae -- NanoDynamics, Inc.; Robert C. Pfahl and Charles Richardson .... iNEMI

Development and Characterisation of Micrometer-Sized Polymer Particles with Extremely Narrow Size Distribution
H. Kristiansen and K. Redford .... Conpart AS
Z. Zhang and J. Hee .... NTNU
M. Fleissner , P.I. Dahl ... SINTEF Material and Chemistry

High Performance Non-Conductive Film (NCF) with Conjugated Molecular Wires
Yi Li, Myung Jin Yim, Kyoung Sik Moon, and C.P. Wong
.... Georgia Institute of Technology

Characterization of Effective Chemical Shrinkage and Modulus Evolution During Polymerization
Yong Wang and Bongtae Han .... University of Maryland

On the Study of Parylene-N for Millimeter-Wave Integrated Circuits
Rosa R. Lahiji, Hasan Sharifi, and Saeed Mohammadi –
....Purdue University
Linda P.B. Katehi .... Univ of Illinois, Urbana-Champaign

——— SESSION 6: 1:00 PM – 4:45 PM———

Joint IEMT-APM: Poster Session

Session Co-Chairs: Ed Aoki, Agilent (retired), Dr. Vasudeva Atluri, Intel

Case Study on the Validation of SAC305 and SnCu Based solders in SMT, Wave and Hand-Soldering at the Contract Assembler Level
Peter Biocca .... Kester
Carlos Rivas .... SMT Dynamics

Effects of Postbake on the Microstructure and Whisker Growth of Matte Sn Finish
Chong-Hee Yu and H.S. Kang
.. Electronics and Telecommunications Research Institute
Kyung-Seob Kim .... Yeojoo Institute of Technology
Sung-Won Han, Kyung-Chun Yang
.... Chung-Ang University

A Study of the Rheological Properties of Lead Free Solder Paste Formulations used for Flip-Chip Interconnection
Sabuj Mallik, Ndy Ekere, Antony Marks
.... University of Greenwich at Medway, UK
Rajkumar Durairaj
.........University Tuanku Abdul Rahman (UTAR), Malaysia

Eutectic Liquid in Sol-Gel Process for Superhydrophobic Silica Thin Films Antistiction of MEMS Devices

Yonghao Xiu, Lingbo Zhu, Dennis W. Hess, and C.P. Wong Georgia Institute of Technology

Three Dimensional Mold Flow Analysis for Stacked Die Package During Injection Molding Process For Stacked-Die Packages
Sung-won Moon, Cheng Yang, Zhihua Li, and Anthony Fischer .... Intel Corp

Work Instructions and Assembly Documentation: Doing It Right the First Time
Terry Chappell .... Chappell Enterprises Corp.

High-k Polymer Nanocomposites for Gate Dielectric Applications
Jiongxin Lu, Kyoung-Sik Moon and C.P. Wong
.... Georgia Institute of Technology

Optimization of Nickel Thickness on Substrate for TBGA using SAC387 Solder Material
Ibrahim Ahmad, B.Y. Majlis, A Jalar
.... Universiti Kebangsaan Malaysia
Eu Poh Leng....... Freescale Semiconductor (M) Sdn. Bhd

Effect of Silica on the Non-Linear Electrical Property of Polymer Composites
Guseul Yun, Yangyang Sun, Fei Xiao, Kyoung-Sik Moon, and C.P. Wong .... Georgia Institute of Technology

Fluxless Bonding of Si Chips to Ag-Copper Using Electroplated Indium and Silver Structures
Jong S. Kim, Pin J. Wang, Chin C. Lee .... UC Irvine

Thursday, October 4, Reception

5:00 PM – 7:00 PM
Sponsored by the Exhibitors.
Held on the patio, with a Western USA theme.
Featuring the '60's – '80's rock band, Silicon Cowboy.
Raffle (prizes include 2 XBox360's donated by Microsoft)
Included in registration fee
Guest Tickets available for $40

Thursday, October 4 – Evening

8:00 PM: Chapter meeting, Lasers & ElectroOptics Society
"Compact High-Repetition-Rate Soft X-ray Lasers"

Friday, October 5, Morning

——— SESSION 7: 8:00 AM – 11:40 AM———

APM: Materials for Interconnects

A Novel Ag-Cu Lamination Process
Pin J. Wang, Jong S. Kim, Chin C. Lee .... UC Irvine

Characterization of a Thick Copper Pillar Bump Process
Warren W. Flack, Ha-Ai Nguyen .... Ultratech, Inc.
Elliot Capsuto, Craig McEwen ..... Shin-Etsu MicroSi, Inc.

Flip Chip Solder Bumping by Newly Developed Ball Mounting Method
Koji Sato, Shigeharu Uematsu, Motoki Wakano, Masaru Fujiyoshi, Nobuhiko Chiwata .... Hitachi Metals, Ltd.

Pull Strength Evaluation of Sn-Pb Solder Joints Made to Au-Pt-Pd Conductor on Low-Temperature Co-Fired Ceramic
P. Vianco, F. Uribe, G. Zender - ....Sandia National Labs

SESSION 8: 8:00 AM – 11:40 AM

Joint IEMT/APM: Lead-free Soldering and Bonding

Session Co-Chairs: Vikas Gupta, Texas Instruments, and John Pan, Cal-Poly San Luis Obispo

The Effect of Ni Thickness on Mechanical Strength of Pb-Free BGA Spheres on Selectively Plated Ni/Au Finish
Poh Leng Eu .... Freescale Semiconductor Malaysia
Min Ding,Joah Rayos .... Freescale Semiconductor, Inc.
Ibrahim Ahmad and Azman Jalar
.... National University of Malaysia
Cheng Qiang Cui .... Compass Technology Co., Ltd.

Development Status of High Speed Ball Pull for Pb-Free BGA Characterization
Paul Hundt and Vikas Gupta .... Texas Instruments

Characterisation of 980nm Pump Laser Solder Joint Integrity Using Heat Pump Tests
G Takyi
.... Kwame Nkrumah Univ of Science and Technology
C. Beesley, A. Kendal, R. Baettig .... JDS Uniphase

Pb-free BGA Solder Joint Reliability Improvement with Sn3.5Ag Solder Alloy on Ni/Au Finish
Poh Leng Eu .... Freescale Semiconductor Malaysia
Min Ding, Wayne Lindsay, Sheila Chopin
.... Freescale Semiconductor Inc.
Ibrahim Ahmad, Azman Jalar ... National Univ of Malaysia

Pb-free Solder: SAC105 vs SAC305 Drop-Test Reliability Data Comparison
Ganesh Iyer, Eric Ouyang, Witoon Kittidacha, Soratos Tantideeravit, and Suresh LK .... Spansion Inc.

Treated Lead-Frame for Leaded Plastic Molded Package
Shutesh Krishnan, Y.S. Won, and K.Y. Lau
.... ON Semiconductor

Method of Making Low-Cost Multiple-Row QFN
Mary Jean Ramos, Rico San Antonio, Lynn Guirit, Anang Subagio, Hadi Handoyo .... Unisem Singapore

Exhibits Open: 9:30 AM – 3 PM

APM Symposium Luncheon, sponsored by Flextronics
Luncheon speaker: "Thinking Outside the Box", Dr. William Chen, ASE, &CPMT Society President
Final Raffle Prize-winners selected

Friday, October 5, Afternoon

SESSION 9: 1:30 PM – 5:00 PM

IEMT: Packaging for MEMS, 3D, WLP

Session Co-Chairs: Wan-Thai Hsu, Discera, Charles Yang, Miradia

Ceramic Package Solutions for MEMS Sensors
Adam Schubring .... Kyocera America, Inc
Yoshitsugu Fujita .... Kyocera Corporation

Low Cost Packages for MEMS Oscillators
Wan-Thai Hsu .... Discera, Inc.

Challenges and Solutions for Cost-Effective RF-MEMS Packaging
Art Morris and Shawn Cunningham .... Wispry, Inc

Through Wafer Via Technology for MEMS and 3D Integration
Magnus Rimskog .... Silex Microsystems

Flexible Design Techniques for a Polysilicon MEMS Process
Andrew McNeil -- Freescale Inc.

Wafer Level Hermetic Packaging of MOEMS Devices
Charles Yang, Antai Xu, and Ye Wang .... Miradia, Inc

Warpage Modeling and Characterization to Simulate the Fabrication Process of Wafer-Level Adhesive Bonding
Ji-Hyuk Lim, Suk-Jin Ham, and Byung-Gil Jeong
.... Samsung Advanced Institute of Technology

SESSION 10: 1:30 PM – 5:00 PM

APM: Nanotechnology

Session Co-Chairs: Alan Rae, NanoDynamics Inc., CP Wong, GaTech

State-of-the-Art Photonic Nanostructure Devices
Toshihiko Baba .... Yokohama National University

Fine-Pitch Carbon Nanotube Bundles Assembly Using CNT Transfer For Electrical Interconnects
Lingbo Zhu, Kyoung-Sik Moon, Dennis W. Hess, and C.P. Wong .... Georgia Institute of Technology

First-Principles Simulation Study on the Effects of Dopants on the Cohesion of Gold Grain Boundary
Y.H. Chew, Z. Bakar, J. Ling ... Kulicke and Soffa (S.E.A.)
C.C. Wong .... Nanyang Technological University

In-Situ Thermal Deformation Measurement of Low-k layer Using Nano-Pattern Recognition and Correlation Technique
Hongbo Bi and Bongtae Han .... University of Maryland

Tin/Silver Alloy Nanoparticles for Low-Temperature, Lead-Free Interconnect Applications
Hongjin Jiang, Kyoung-sik Moon, and C.P. Wong
.... Georgia Institute of Technology
Fay Hua .... Intel Corp.

SESSION 11: 1:30 PM – 5:00 PM

Joint IEMT/APM: Design for Environment

Session Co-Chairs: Allen Amaro, Hong-Chao Zhang, Texas Tech University

European Environmental Legislation - Insights into the EuP Process
Nils F. Nissen, Lutz Stobbe, Karsten Schischke, and Jutta Müller .... Fraunhofer IZM
Herbert Reichl .... Technical University of Berlin

Impact of New Materials and Processes on Manufacturing: Green (Pb and Halide-Free), ROHS Experience
Chandru Idnani .... Enterprise Consulting

Integrating Energy-Saving Concept into General Product Design
Hua Li, Hong-Chao Zhang, John Carrell, and Derrick Tate
.... Texas Tech University

Repeatability Analysis of EDXRF Equipment for RoHS Compliance Screening for Soldering Materials Used in PCBA Manufacturing
Jasbir Bath, Roger Jay, Leonora Bennett, Suan Kee Tan, Pan Wei Chih, Adrian Lucuta .... Solectron Corporation

Challenges in the Assembly of Large Die, High Bump Density Pb-Free Flip Chip Packages
Jeremias Libres, Karen Robinson .... Texas Instruments

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Persons with a disability: Requests for accommodations for persons with disabilities are due to Paul Wesling, conference administrator, by 24 September. My special needs/requirements include

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Morning Course (choose no more than one)
- ☐ **Nanotechnology Applications in Packaging**, Florin Ciontu
- ☐ **Implementing Flip Chip & WLP Technology,** Peter Elenius
- ☐ **Advanced Packaging Technology Solutions for Today's Leading Edge Microelectronics**, Charles Woychik, GE
- ☐ **Achieving High Reliability for Lead-Free Solder Joints - Materials Considerations**, Dr. Ning-Cheng Lee, Indium Corp

Afternoon Course (choose no more than one)
- ☐ **Polymers & Nano-Composites in Electronic, Opto-Electronic and Photonic Packaging**, Dr. CP Wong, GaTech
- ☐ **3-Dimensional Semiconductor Packaging & Integration,** Dr. Charles E. Bauer and Dr. Herbert J. Neuhaus
- ☐ **Failure Modes & Analysis of Flip Chip Assemblies**, Prof. Daniel Baldwin, GaTech

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