

"SOP vs SiP vs SOC: Technology Directions for Systems Implementation" Emerging and Disruptive Packaging Technologies for the Next Decade

Wednesday, May 4, 2005, from 8:00 AM - 5:30 PM



Featuring the technical staff of the NSF-sponsored Georgia Tech Packaging Research Center held at the Ramada Inn, Sunnyvale

Register Early to assure a seat
(we expect this to fill up)

DATE & TIME: Wednesday, May 4
8:00 AM - 5:00 PM
Registration: 7:30 AM
Lunch: Noon - 1:15 PM
Reception/dinner following: 5 - 8 PM

LOCATION: Ramada Inn, 1217 Wildwood
Ave (101 and Lawrence), Sunnyvale

COST:

IEEE Members: \$95
Non-Members: \$150
(after April 25: Member \$110,
Non-Member \$165)

Includes lunch, refreshments, class
booklet, and admission to the
optional evening reception & light
dinner

WHO SHOULD ATTEND:

Packaging engineers, photonics
engineers, systems engineers, thermal
and mechanical engineers, PCB layout
engineers, design, process, failure
analysis, and reliability engineers.

INFORMATION, OR TO REGISTER:

Please register and pay concurrently,
using our PayPal system at

www.cpmt.org/scv/

To pay by mail, please print the form below
and send with your check (no credit cards,
please).

For additional registration information, or to
check for status, contact Janis Karklins, (408)
374-0960.



IEEE COMPONENTS, PACKAGING AND
MANUFACTURING TECHNOLOGY SOCIETY

Morning Session (8:00-11:45AM)

"**SOP: The Second Moore's Law for Systems in Contrast to First Moore's Law for ICs**," Prof. Rao Tummala, Director, GaTech Packaging Research Ctr
"**Mixed Signal SOP Design**," Prof. Madhavan Swaminathan - System on a Package solutions - heterogeneous functions: RF, Digital, Optoelectronics - coupling: analog-analog, digital-analog, digital-digital - managing signal integrity, power integrity, EMI control - design tools, methodologies - design approaches, design tools, new technologies

"**High-Density/High-Throughput Chip-to-chip Optical Interconnect SOP for Next-Generation Computing and Communication Systems**," Prof. Gee-Kung Chang - Motivation for optical interconnect (OI) systems - High speed performance of electrical vs. optical wiring - Optoelectronic SOP Roadmap - OI Design - OI layout - Optical passives - Embedded actives - Embedded devices - Thick film lasers and photodetectors - End-to-end integration and testbed results - Future trends and challenges

"**RF/Wireless 3D Packaging and Integration: Current Challenges and Solutions**," Prof. Manos Tentzeris - Quality (Q) factor and loss mechanisms in embedded passives - Vertical Interconnects (Flip-Chip, BGA, PGA) - Embedded Components - 3D Multilayer Passives, Functions and Modules - Packaging Adaptive Antennas - Integrated Wireless Transceivers - RF-MEMS - full-wave simulation tools (e.g. FDTD) - Practical designs using modeling CAD tools

12:00: Buffet Lunch (seating); 12:15 - 1:00: Keynote Presentation: "**US and Electronic Industry Competitiveness in view of Globalization and Changing Technologies**," Prof. Rao Tummala - IC and Systems Packaging: the electronics stepchild - IC packaging, component fabrication, assembly - RF, digital, optical, MEMS sensors, fluidics, nano, bio systems - Nearly as large as the IC market - Japan, Taiwan, Korea, China - fundamental integration limits: consumer and medical electronics - short term solutions: SIP and SOP - University de-emphasis - Source for new breed of engineers - Competitiveness of US industry

Afternoon Session (1:30-5:00PM)

"**High Performance Nano Materials for Electronic, Photonic and MEMS Packaging**," Prof. C.P. Wong

"**Multigigahertz Test Methods for SOPs and Wafer-level Packaged Devices**," Prof. David Keezer - Test Support Processor - Digital Test Core Electronics - 5 Gbps Wafer Level Prober - Test Methods for Optical Switching Networks - Test Support Electronics for ATE - Future Directions

"**Thermo-Mechanical Reliability and Design Challenges for Next-Generation Microsystems Packaging**," Prof. Suresh Sitaraman - challenge of reliability - moving to 1 billion-transistor ICs - Shrinking IC feature size - thermo-mechanical reliability, design challenges - area-array flip-chip and ball-grid array packages -time-, temperature-, and direction-dependent modeling - predictive reliability models - Failure modes (solder joint creep, fatigue damage, delamination, die and microvia cracking)

5:00 - 8:00: Informal Reception and Social with Drinks and Light Dinner
Meet the Georgia Tech PRC faculty members for informal discussions

HOW TO REGISTER:

FEES: IEEE Members: \$ 95 (\$110 after April 29)
other attendees: \$150 (\$165 after April 29)

(includes class handbook and refreshments)

Checks or P.O.s should be made payable to "IEEE/CPMT"
and sent with the completed registration form below to:

Janis Karklins
2671 La Salle Way
San Jose, CA 95130
(408) 374-0960

Limited Seating. Register by EMAIL NOW to reserve your seat!
Your registration will be CONFIRMED when payment is received.
Checks and Purchase Orders should be made out payable to "IEEE-CPMT".
Credit Card Payments Through PayPal Only -- see above.

REGISTRATION FORM

SOP vs SiP, vs SOC: Technology Directions for Systems Implementation
Wednesday, May 4, 2005, 8:00 AM - 5:00 PM

Email your Registration Form to: Janis Karklins or mail to:
2671 La Salle Way
San Jose, CA 95130

Make Checks and Purchase Orders payable to "IEEE-CPMT".

Credit Card Payments Accepted Only Through our Online PayPal Account (above)

Payment and cancellation refund requests due by Friday April 29.
Substitute attendees accepted anytime. Attach list of other
individuals you are registering and include payment.

NAME _____ COMPANY _____

ADDRESS _____ JOB TITLE _____

CITY _____ STATE _____ ZIP _____

Phone _____ Include FAX# for Confirmation _____

Email _____

Payment by:

Check # _____ PayPal _____ P.O. _____

Amount \$ _____ IEEE Mem.# _____ (Required For Discount)

If you can't attend, what about a Team Member?