IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Summer-Fall 2010
Volume 1, Issue 2

SANTA CLARA VALLEY CHAPTER NEWSLETTER

Components Packaging and Manufacturing Technology - Santa Clara Valley Chapter
www.cpmt.org/scv cpmt@ieee.org Editor: Joseph Fjelstad - contact - j.fjelstad@ieee.org

Message from the Chapter Chair

By Ed Aoki

Greetings CPMT members and friends,
The first half of 2010 has been very busy and eventful. We have thus far had 8 excellent technical program events at the Biltmore this year including 6 dinner meetings and 2 lunch meetings. The slide sets for most of these presentations are available through links at www.cpmt.org/scv. For the balance of 2010, we have 4 Technical Programs committed for September - November. These are also described at www.cpmt.org/scv .

To support our members, we now offer a 50% discount for students and unemployed IEEE members on our Technical Program registration page.

In May of this year, we co-sponsored the IEEE-SFBA-Nanotechnology Council Symposium which is an area of growing interest to a number of CPMT and other IEEE technologists.

You'll remember that IEEE-SCV-CPMT supports the San Jose State University CPMT Student Chapter which is growing and has received financial support from both the IEEE SCV Section and our Chapter. We recognized the efforts of Reuben Thibodeau, the 2009-2010 Student Chapter Chair, by sponsoring his attendance at ECTC 2010 in Reno, NV.

INSIDE THIS ISSUE

PAGE

Chairman's Message (continued from left)

I have a question for you… **Are you an IEEE Senior Member?** Not yet, you say? Would you like to join the 8.7% of the IEEE membership who are Senior Members? You may well already be eligible**.** The IEEE assigns an education credit of 5 years for a PhD, 4 years for an MS/MA/MBA and 3 years for a BS/BA. If you have been working for 5 to 7 (or more) years and have a total of 10 years (Education credit + work experience), you are probably eligible for elevation to Senior Member Grade. Contact Luu Nguyen < l.nguyen@ieee.org > or Ed Aoki < e.aoki@ieee.org > for application details.
Also If you are an IEEE Senior Member or an IEEE Fellow and are willing to volunteer some time in reviewing applications and resumes of applicants for elevation to SM grade, please contact Ed or Luu at the addresses above.♦

SCV and Malaysia CPMT Chapter Sisterhood Bonding Continues

By Annette Teng

Since 2005, the Santa Clara Valley CPMT Chapter has played a big sister role to the then fledgling Malaysian Chapter. This "sisterhood" was the brainchild of Dr. William Chen and our CPMT officers including Paul Wesling, Allen Earman, Bernie Seigal, Liz Logan and Annette Teng. To date, the Malaysian CPMT chapter has seen growing membership with members who actively seek to volunteer. From an original core group of OEM companies and University members, they have now expanded to subcontractors and smaller companies. Their membership is much younger in age and well tuned in to the latest technologies. This is the reason why the Malaysian Chapter has produced 2 Outstanding Young Engineer Winners already, including Malaysian Wong Shaw Fong who is the 2010 winner. The CPMT Board of Governors has recognized our sister chapter relationship by presenting both chapters a Certificate of Contribution.
The "sisterhood" was strengthened by way of the IEMT Symposium (International Electronic Manufacturing Tech) moving from Santa Clara Valley to Malaysia. This was a logical decision as the manufacturing sector has dwindled in the US, while growing in Malaysia. C.H.Chew, former Malaysian Chapter Chairman led a team of CPMT volunteers from various Malaysian companies and universities to work together. The first newly located IEMT event was held in December 2006 in Kuala Lumpur and was recognized as the first major IC manufacturing conference in Malaysia. The SCV Chapter helped with the launch by submitting papers and sending speakers. Bernie

Continues in *SCV – Malaysia Sisterhood page 4*

From the Editor's Console

By Joseph Fjelstad

This is the second edition of your newly revived CPMT Santa Clara Valley Chapter newsletter. We are continuing our mission to provide you with a useful resource for information on the activities, workings and opportunities related to both your chapter and the IEEE.

Following the trajectory of information technology and our desire to minimally impact the environment, this newsletter will continue to be available primarily in digital format through email distribution and though a link from our Chapter Web Page (www.cpmt.org/scv). To reach out to those who are not yet members of our society but attend meetings, a few printed copies will be made available at our regular dinner and lunch meetings. Any questions about circulation can be directed to Communications Chairman, Paul Wesling at p.wesling@ieee.org.

As stated here in the last edition, we want to emphasize again that this is your newsletter and while we intend to provide you with content that we believe is important, we are open to your thoughts about new content and are eager to hear from those with interest in contributing news and information that is relevant to CPMT members. As you can see in this edition, the call has been answered by several CPMT members with interesting articles and informative pieces submitted by Annette Teng and Sandra Winkler.

Please feel free to contact me with your ideas, any contributed materials or your criticism. Thank you again for your membership and interest in the CPMT and if you are not yet a member I encourage you to join and take advantage of the many benefits the society offers.

IEEE – CPMT

Santa Clara Valley Chapter

The leading international society for scientists and engineers engaged in the research, design and development of both evolutionary and revolutionary advances in electronic microsystems including their manufacture, packaging and test.

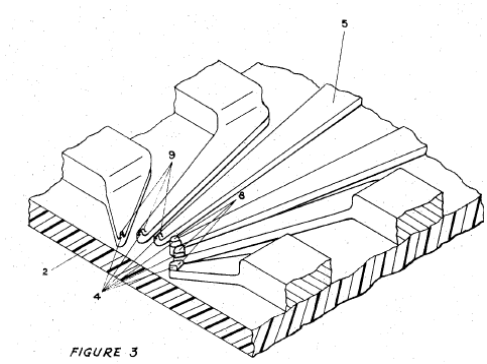
Chapter Officers

Chairman:	Ed Aoki
Vice chairman:	Mudasir Ahmad
Secretary	Dong Ji Xie
Treasurer	Liz Logan
Education chairman	John Jackson
Evening rogram chairman:	Azmat Malik,
Lunch program chairs:	Sandra Winkler, Tom Tarter
Program chairman emeritus	Harvey Miller
Membership chairman	Janis Karklins
Webmaster/Training/Comm	Paul Wesling

E-Mail: cpmt@ieee.org

Electronic Packaging in Santa Clara Valley

In the last edition, we recounted some of the early developments in electronic packaging that occurred in the Santa Clara Valley describing the development of the dual in line package (DIP) by engineers at Fairchild. However, that was just the beginning. Because the Silicon Valley was becoming a hot bed for the semiconductor and the integrated circuit, packaging technology developed along side owing to the fact that, without packaging, the IC was not of much value. Thus there were important packaging solutions conceived in the early days of the integrated circuit industry in the valley that did not get much immediate attention or use but which were later embraced for many important applications and are still broadly used in some specific areas especially displays. The most important of these packaging structures is widely known as TAB technology which was short for tape automated bonding.



A drawing from Santa Clara Valley inventor and pioneering entrepreneur, Frances Hugel

As is often the case with many individuals seeking solutions, near simultaneous invention was the case for TAB. Two inventors of note in the area were Frances Hugel, a pioneering woman engineer and entrepreneur in the field of IC packaging from Silicon Valley. Hugel's stroke of genius was to envision a way to avoid having in interconnect individual wires to the chip by substituting an interconnecting circuit having leads which would connect directly to the chip all at one time and which also fanned out to allow for the assembled device to be mounted on a circuit board. Around the same time across the continent, John Marley of ITT, invented a similar device which was not only TAB like but was among the first to describe what later came to be called a multichip module. Between them they had invented the important elements of TAB technology which found fairly wide popularity for many mid to high pin count ICs in the 1980s. ♦

A Review of ECTC 2010 Las Vegas

By Sandra Winkler,

The 60th annual ECTC (Electronic Components and Technology Conference) drew to a close on June 4th, in Las Vegas, Nevada. Once again, this premier conference didn't disappoint. The conference begins on a Tuesday with professional development courses and an RFID Special Session, and is followed by three full days of technical papers in six tracks being delivered simultaneously. Seven papers are presented in each track for each the morning and afternoon sessions, for a total of 252 technical papers being delivered, plus poster sessions and a technology corner. A variety of topics are presented in the technical sessions, including advanced packaging, interconnection, modeling and simulation, optoelectronics, electronic components & RF, materials & processing, applied reliability, emerging technologies, and assembly & manufacturing technology. Popular topics during the technical sessions include stacking with through silicon vias (TSVs) / 3D integration, non conductive film (NCF) and non conductive paste (NCP), embedded die solutions to create a SiP, and flip chip and interconnection along with many other cutting edge topics. Plenary sessions were both plentiful and excellent.

Tuesday Night's Plenary Session: The Emergence of the Medical Devices Industry through the View-glass of Microelectronic Packaging Innovation

Medical electronics range from diagnostic equipment such as imaging / x-ray to ultra-small devices that are to be inserted within the body. In-the-body implants include hearing aids, retinal implants that aid in restoring some form of vision, spinal implant, ingestible chips that send information wirelessly on how the body is reacting to a given medicine, and an implantable drug pump for time-release of drugs.

Interesting developments include neuro-prosthetics where silicon is fitted with electrodes to interact with the central nervous system, pacemakers,

Continued on page 4

.

Viva ECTC 2010 in Las Vegas - A sizable number of Santa Clara Valley CPMT members were in attendance at this year's event. The SCV CPMT chapter also sponsored Reuben Thibodeau who is Chair of CPMT student chapter at SJSU. In the photo clock wise from the upper left: Li Li, Patricia McLeod, Bill Chen, Jie Xue, Mrs.Theresa Lau, John Lau, Ephraim Suhir, Liz Logan, Sandra Winkler, Paul Wesling, Wong Shaw Fong (Malaysia) and Annette Teng. Also attending but missing at photo shoot: DongJi Xie, Luu Nguyen and Reuben Thibodeau

SCV – Malaysia Sisterhood … continued from page 1

Siegal taught a class on thermal management and Annette Teng taught one on wafer dicing. That first ever Malaysian IEMT conference was very well received and the attendance for classes and sessions beat expectations.

Dr Azhar Aripin representing Malaysian Chapter and Dr. AnnetteTeng representing SCV share a moment on stage at IEMT.

The success of IEMT 2006 propelled the Malaysian Chapter volunteers to become cohesive and worked together organizing regular CPMT activities and a second successful event was held in 2008 in Penang. This coming December will mark the 3rd IEMT conference in Malaysia and will be held in Melaka (see page 9 for details). Like the others this will be well organized and is expected to be opened again with high level government officials in attendance.

Dr. Bill Chen & Azhar Arpin watch as the Chief Minister of Penang strikes a ceremonial gong to open IEMT2008

SCV – Malaysia Sisterhood… continued from left

Attendees have come from the far corners of the globe including many Islamic countries, owing to Malaysia's Islamic history. Engineers and educators from many Muslim communities and nations attend along side engineers from Malaysia and neighboring countries all for the high educational value. Some of the local nations represented include Thailand, Philippines and Indonesia Once again, the December IEMT event will be held in Melaka, location of a historic Portuguese stronghold in Asia. Many SVC CPMT members are looking forward to attending. We hope to see you there ♦

ECTC 2010 Review continued from page 3

neurostimulators to help with Parkinson's disease, infusion pumps for soldiers, biosensors for diabetics that read blood glucose levels, MEMS pressure sensors to sense the body's fluids, and devices to measure intra abdominal pressures and pelvic floor disorders. Robustness and extreme miniaturization are required for devices which need to be inserted or fit within the body. Biocompatibility for devices implanted within the body is necessary. Wireless technology will be used more and more to deliver statistical data from devices implanted in the body to a collection device outside the body available to the doctor and patient.

With soaring medical expenses, bringing down the costs of medical care is vital. Reducing the size of equipment in general will reduce costs, such as creating handheld ultrasound equipment down to the size of a cell phone. The resolution will not be as good, but the device will be portable and low cost. Many of the devices in medical environments are used once and discarded. Cost saving devices may be hybrids, with which multiple uses can be obtained before discarding. In addition, creating standards in medical devices can also lead to reduced costs.

Wafer level packaging, flip chip, SiP, SoC, integrated passives, and 3D integration / TSVs will be used in these markets. Continues on page 7

IEEE Reaches Out to Help Members

In view of the continuing economic turmoil the IEEE, realizing its value of its members is making it possible new or continuing membership during a period of special circumstances which include: unemployment low income, retirement and disability Full details can be found on the web at the link below.

http://www.ieee.org/web/membership/Cost/special_circumstances.html

Technology Corner

New worldwide IC packaging market study available

The semiconductor industry has been cyclical since its inception, but the general trend for the industry continues upward according to a newly released report, The Worldwide IC Packaging Market, 2010 Edition. The report provides an in-depth look at the integrated circuit (IC) packaging market worldwide, forecasting individual IC device markets for units, revenue, and ASP, from 2008 through 2014. Package solutions for each of the forecasted markets are broken down into I/O ranges. Package types are rolled up In one chapter to deliver an overall worldwide forecast of IC packages, divided into 12 different package families, plus bare die solutions. The major package families include:

- Dual in-line package (DIP)
- Small outline transistor (SOT)
- Small outline (SO)
- Thin small outline package (TSOP)
- Dual flat pack no lead (DFN)
- Chip carrier (CC)
- Quad flat pack (QFP)
- Quad flat pack no lead (QFN)
- Pin grid array (PGA)
- Ball grid array (BGA)
- Fine-pitched ball grid array (FBGA)
- Wafer-level package (WLP)

Additionally, unit forecasts for die mounted using direct chip attach (DCA) methods were developed. DCA methods include chip on board (COB), flip chip on board (FCOB), chip on glass (COG), flip chip on glass (FCOG), and tape automated bonding (TAB)/tape carrier package (TCP).

The contract IC packaging market is reviewed and projected and units and revenue are analyzed by package family. Forecasts are computed by compiling information obtained from each individual contract assembly company. .

The report is offered to aid companies associated with the IC packaging anticipate demand for their own products. The IC packaging market is evolving to keep pace with other changing markets. IC packaging demand is affected by changes in the die contained in the packages, and by performance expectations of the final product purchased at the consumer level. Through extensive primary and secondary research, this report presents an objective look at the world of IC packaging.♦

Visit www.newventureresearch.com or contact Karen Selven Williams@ kwilliams@newventureresearch.com.

Economic Picture is Looking Better

By Sandra Winkler, New Venture Reesarch

IC revenue will grow at 18.8% in 2010, with unit growth at 18%, according to New Venture Research (formerly Electronic Trend Publications), considerably better than the 8.8% decline in revenue and 6.9% decline in units in 2009. DRAMs are anticipated to be the largest growth area for ICs, with 40% revenue growth in 2010. Analog chips, including regulators & references, computer, communications, automotive, and industrial applications; special purpose logic chips including consumer, computer, communications, and automotive; flash, EEPROM, 32-bit MCU, and standard cell and PLD chips will all see revenue growth rates in excess of 15%.

Lower interest rates, lower oil prices, and the stimulus packages that were instituted around the world are all contributing to a stabilizing economy and upturn. Purchases were less than the replacement market in 2009, and pent up demand is pulling the market in a positive direction.

Cell phones, especially the high-end smart phones, will see high growth rates. Smart phones are gaining in popularity and are becoming a larger piece of the cell phone pie. Anything handheld and somewhat affordable that keeps us connected to the rest of the world seems to be doing well. New product introductions such as Apple's iPhone and iPad are doing well, along with the Blackberry by Research in Motion (RIM).

Netbook computers, with prices near $200 and notebook computers are driving up IC demand. Other high growth areas include 3D and digital TVs, DSL/ cable modems, flash drives, memory cards, set top boxes, digital cameras, automotive, and an assortment of audio applications.

The economy has been stabilizing, which is easing some fears over spending on consumer goods. The housing market, which took down the economy by taking the credit markets down with it, is stabilizing, and the ratio of income to housing expenditure is more balanced than it was previously. The automotive market, which consumes numerous ICs, had fallen substantially during the downturn but is returning slowly. The market did benefit from the cash-for-clunkers program, but sales fell back after the program ended. Still it did bolster some spending, which helped. Automotive is expected to turn up for the year, particularly in areas such as China. Overall, spending is higher now than it was in the depths of 2009. And that is what is pulling up and out of the sloth of 2009, and will carry us to a more positive future.

For more information contact the author at NVR.♦ (www.newventureresearch.com)

Meetings You May Have Missed

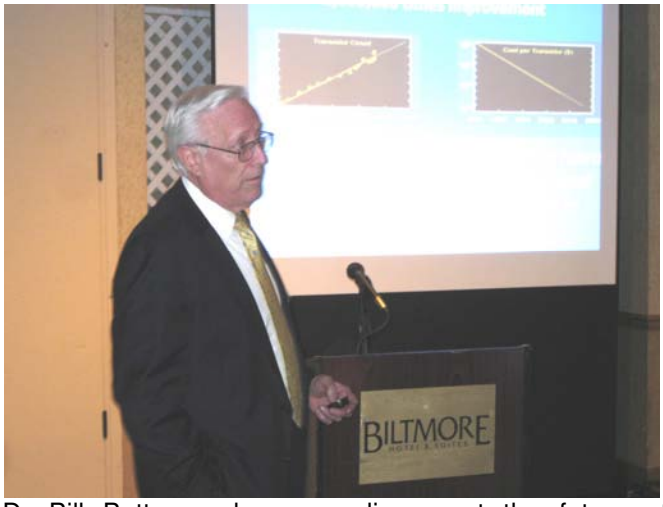
The Santa Clara Valley chapter of the IEEE CPMT Society is among the most active in the world and is constantly striving to provide valuable information in a timely manner. Much of the credit for the success of the meetings rests at the feet of our outstanding programming team, co-chairs Azmat Malik and Sandra Winkler assisted by Harvey Miller. Following is a sampling of some of the outstanding presentations to which members have been treated this year.

"3D IC Integration: The Next Generation of Electronics" -- Dr. W. R. Bottoms, Chairman, Third Millennium Test Solutions (3MTS)

"Integrated RF-CMOS MEMS Solutions for Mobile Terminals"
- Jeffrey L. Hilbert, President, WiSpry, Inc. (Irvine, CA)

"Winner Take All: How Competitiveness Shapes the Fate of Nations",
Presented by the author, Richard J. Elkus, Jr

For more information and to view slides visit the CPMT website at:
http://www.cpmt.org/scv/



Dr Bill Bottoms shares a glimpse at the future of electronic packaging with CPMT members and guests at a dinner meeting in March

Up Coming Meetings

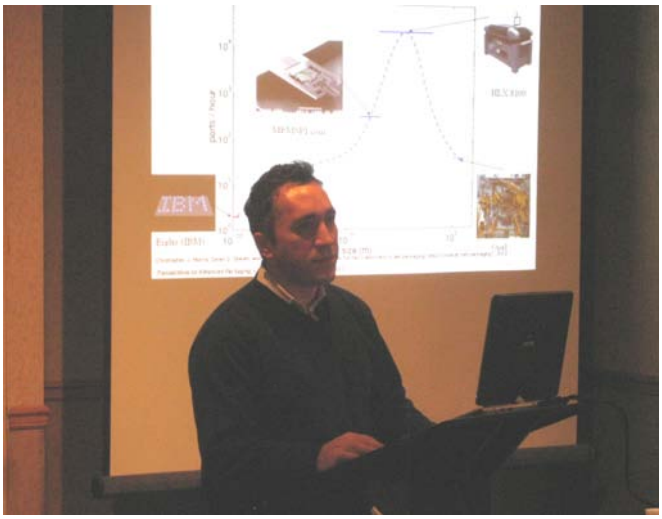
Continuing to provide educational opportunities to its members, your CPMT chapter has lined up an outstanding program with top tier speakers and timely topics for the fall. Below is a sampling of some of what is on tap. Mark the dates!

"Design of High Density & 3D Packaging: Tools and Knowledge"
-Thomas Tarter, Package Science Services LLC
Lunch meeting Thursday, September 23, 2010

"All-Silicon System with Nano-Packaging: Highest Functionality, Lowest Cost, Smallest Size"
-Prof. Rao Tummala, Founding Director, NSF Packaging Research Center, Georgia Tech
Dinner meeting Tuesday, October 12, 2010

"Good Things Come in Small Packages"
- Sandra Winkler, New Venture Research
Lunch meeting Thursday, October 28, 2010 **(postponed)**

"Embedded Passives: Packaging Paradigm of the Future?"
-Jason Ferguson, Crane Naval Surface Warfare Center
Dinner meeting Wednesday, November 10, 2010



Professor Babak A. Parviz of the University of Washington talks on self-packaging of microscopically small electronic components and their applications

Want the Latest Schedule of CPMT Events? Seminars and Short-Courses? Check out our Web Page at www.cpmt.org/scv.
*For CPMT and all SF Bay Area IEEE Chapter Events go to the **eGRID** at http://e-grid.net/*

ECTC 2010 Review continued from page 4

More development is needed in the packaging area, as the packaging solutions are not keeping up with the advancements in silicon now. Battery power is also not keeping up with current needs and there will be further demands from the industry. Future challenges will include stretchable substrates with sensors attached to go on shoes or an ace bandage.

Wednesday: Semiconductor Business Evolution

The luncheon speaker was Dr. Tien Wu of ASE Group, speaking about semiconductor business evolution. The growth rate within the semiconductor industry is 6 to 7 percent, and is greater than the growth in GDP, which is quite positive. For an individual company to obtain a larger growth rate, it must steal business from competitors, which leads to price wars. The industry invests $1 billion more in the front end than in the backend, which means the backend is lagging. Investment in the backend will catch up over the next ten years. The growth in the semiconductor industry has come in waves focused around specific industries. The PC wave included CPU, memory, and storage devices, followed by communications, and connectivity, bandwidth, and people-to-people communications, information and life sciences appears to be the next. Each wave is higher than the one behind it, meaning more money is to be made in each successive wave.

There are three strategic business plans or directions to take, which are: 1) The Long Tail - Older technology with lower margins. 2) Hyper Jump - New technology with higher margins. 3) New Region - Adopt new technology to local ecosystems or new locals.

His closing remarks included mentioning that China will or should become the largest consumer economy in the world, surpassing the United States.

Wednesday Night Plenary Session:

In this session *"*The Evolution of Mobile Processing Architectures*"* 4G mobile phones of the future were discussed (we are at 3.9G currently). These phones will have data transmission speeds of 50 Kbps (uplink) and 100 Mbps (downlink), which means that increased speeds will be needed from baseband processors. Like the medical industry, mobile devices will require increased battery life, and running the everyday functions will have to consume less power.

While once the corporate market was driving the demands on smart phones, now the consumer market is driving applications. The user interface is thus critical; that is, human centered. MEMS microphones will be incorporated into smart phones. Global video streaming will in incorporated into 90 percent of smart phones in the future. Mobile devices must be cloud ready, which allows for unlimited computing capacity.

continued on right

There is an obsession to getting cell phones as thin as possible, with IC package height at 1 mm a holy grail. Through silicon vias (TSVs) are already in camera phones now, incorporated within CMOS image sensors. Qualcomm will be introducing a chip soon that will have TSVs and microbumps with flip chip. Via middle (through silicon vias made in the middle of wafer processing) is taking precedence over via first or last. Stacking using chip to chip bonding (rather than wafer-to-wafer or die-to-wafer) will be used when a large memory is being stacked with a processor. The dissimilar size of the two dies dictates this.

Meanwhile, FBGAs have 0.4 mm pitch and a pitch of 0.3 mm is on the way with pin counts up to 1,000 I/O and more. Packaging changes will have to accommodate low k and lower k dielectrics, shift from wire bond to fine-pitch flip chip to copper pillars, and be lead, bromine, and chlorine free. The baseband module will require shielding, and the RF and digital will have to be partitioned. A deep understanding will be needed of use conditions. New failure mechanisms can be expected, not just from the individual elements that must be incorporated within each cell phone, but the interactions of the individual elements.

Thursday Night Plenary Session

"Advanced Bump and Bump-less Interconnection Technologies" was the topic. Non conductive film (NCF) is needed for wafer level packaging when attaching and bonding a glass substrate. The bumps on the wafer displaces the film to achieve electrical connection, and the bump would have a resin core.

When stacking with TSVs, the vias are drilled through the bottom die to interconnect the top die to the substrate below the lower die. Ultra-fine bumps or copper posts are needed for flip chip, with Sn/Ag (tin silver) solder, which would be underfilled. No cleaning is required before reflow, and the IMC (intermetallic compound) is easier to control.

One speaker discussed creating fine bump joints for TSVs for high speed signal transmission; gold (Au) bumps, or cylinder posts, of 5, 10, or 20 µm are used. Electroless plating is used, a wet fabrication process. Vias are created of 10 µm high, 5 to 20 µm in diameter, with a 30 µm pitch.

Networking Opportunities

Networking opportunities are always an important part of any conference, and a chance to feel the "pulse" of what is happening and what is important to the industry.

A total of 844 attendees came to Las Vegas this year; be sure to be counted at the 61st ECTC next year in Orlando, Florida's Walt Disney World Swan and Dolphin Resort, May 31 through June 3, 2011. ♦

http://www.cpmt.org/proceedings/order.html for more info or contact Paul Wesling at p.wesling@ieee.org.

Coming Events - SEMI-THERM 2011, San Jose, CA

SEMI-THERM 27

Thermal innovations that make the world's technology cool

27th Annual Semiconductor Thermal Measurement, Modeling and Management Symposium

Doubletree Hotel San Jose, CA US
March 20-24, 2011

SEMI-THERM is the premier international forum dedicated to the thermal design and characterization of electronic components and systems. The symposium fosters the exchange of knowledge between practitioners and leading experts from industry, as well as the exchange of information on the latest academic and industrial advances in electronics thermal management. We encourage you to submit an abstract on your latest modeling, designs, and results. Online submission of abstracts will be open soon at www.semi-therm.org.

What to expect at SEMI-THERM 27:

- Short Courses from leaders in thermal management and cooling technology
- Keynote Speaker - Forward looking issues in thermal management, markets and needs
- Multiple single-track and parallel technical sessions
- Vendor Exhibits and Workshops
- Industry and Academia Panels
- Awards Luncheon - Best Paper, THERMI and Harvey Rosten Engineering Excellence Award



For more information and call for papers:
www.semi-therm.org
ttarter@semi-therm.org

SEMI-THERM®

Coming Events – IEMT 2010, Melaka, Malaysia

Visit http://ewh.ieee.org/r10/malaysia/cpmt/iemt.htm for more information

A. **IEMT2010 SHORT COURSES -**

1. Title : State-of-The-Art and Trends in 3D IC/Si Integrations and WLP.
   Leader : **Dr. John H Lau**, ITRI, TAIWAN

2. Title : Advanced Copper Wire Bonding Technology.
   Leader : **Dr. Ho Hong Meng**, Semicon Fine Wire, SINGAPORE

3. Title : Past, Present and Future of Electronic Packaging.
   Leader : **Joseph Fjelstad**, Verdant Electronics, USA

4. Title : Flip Chip Technology
   Leader : **Dr. Yutaka Tsukada**, Ritsumeikan/Osaka University, i-PACKS, JAPAN

B. **IEMT2010 KEYNOTE SPEAKERS -**

1. Title : Heterogeneous Integration – A Key Enabling Technology.
   Speaker : **Dr. Rolf Aschenbrenner**, Fraunhofer Institute, GERMANY

2. Title : The Practice of Engineering in The Year of The Tiger.
   Speaker : **Dr. William Chen**, ASE, USA.

3. Title : Automotive Electronics – Packaging As Enabler Technology.
   Speaker : **Dr. Andreas Knoblauch**, Infineon, GERMANY

4. Title : Innovation & Collaboration - Keeping up with Market Demands & Transitions.
   Speaker : **Mark Brillhart**, CISCO, USA

5. Title : Importance of Reliability In Electronics.
   Speaker : **Joseph Fjelstad**, Verdant Electronics, USA

6. Title : Current Technology Barriers and Future Direction for Packaging Density Increase.
   Speaker : **Dr. Yutaka Tsukada**, Ritsumeikan/Osaka University, i-PACKS, JAPAN

7. Title : IC Test Technology Development.
   Speaker : **CS Liu**, National Semiconductor, USA

8. Title : Packaging Trends in Mobile Electronics, Towards Wafer Level Packaging.
   Speaker : **Xavier Baraton**, ST Microelectronics, SINGAPORE

C. **IEMT2010 INVITED PAPER -**

1. Title : Evolutionary Development of Wafer Level Packaging
   Speaker : **John Hunt**, ASE Inc, USA

2. Title : DFMEA/PFMEA : What They Never Teach You In formal School.
   Speaker : **Shankar Shridhar**, EQIS, Australia

3. Title : Ultra Low CTE (0 ppm/C) Polyimide Film and its Potential Application
   Speaker : **Dr. Yutaka Tsukada**, Ritsumeikan/Osaka University, i-PACKS, JAPAN

4. Title : Miniaturization Innovation Evolution of Electronics Packaging – What's Coming Next …?
   Speaker : **Amir Nur Rashid Wagiman**, Intel Technologies, MALAYSIA