



IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Summer 2011
Volume 1, Issue 2

SANTA CLARA VALLEY CHAPTER NEWSLETTER

Components Packaging and Manufacturing Technology - Santa Clara Valley Chapter
www.cpmpt.org/scv cpmt@ieee.org Editor: Joseph Fjelstad - contact - j.fjelstad@ieee.org

Message from the Chapter Chair

By Mudasir Ahmad

The first half of 2011 has been very busy and eventful. Our technical programs continue to draw interested audiences as we continue in our effort to provide topical information for members of the Santa Clara Valley CPMT chapter and the larger electronics engineering community as well. As usual, the slide sets for most of our past presentations are available through links at www.cpmpt.org/scv. This year, we have also started recording some of our technical presentations live (audio) and posting them on our website allowing members listen to the presentations along with the insightful discussions and comments of the audience. We have also organized field trips at local facilities of interest to our members (see the Whizz Systems piece in this edition). We plan to provide more top notch programming as a tribute to those who established the tradition.

There is good news to share about the chapter: once again our efforts have been noted and we have been recognized as the CPMT Chapter of the Year by the IEEE SCV Section. Congratulations to all of those who made it possible. We all know that the industry has not yet fully recovered and thus we plan to continue to support our members by offering a 50% discount for students and unemployed IEEE members on our technical program registration page. You should know

Personal Reflections on IEEE Membership

By Daniel N. Donahoe, PhD, PE

Introduction

The purpose of this article is to answer a question often asked by new engineering graduates. The answer to this question bedevils officers in IEEE. The question is "How does IEEE benefit me?"

The best answer to such an open-ended and very personal question is provided by a case study, a common pedagogical approach used in business school. I will use my own experience as the basis of a case study.

Let me begin this short article with full disclosure: I am an electronics engineer rather than an electrical

INSIDE THIS ISSUE

PAGE

Message from the Chapter Chair	1
Reflections on IEEE Membership	1
From the Editor's Console	2
Electronics Packaging History in Santa Clara Valley	2
MicroMouse Competition	3
ECTC and the Future of Engineering	5
IC Packaging continues to Blossom	6
Dinner and Lunch Meetings Info	7
Whizz Systems Open House for IEEE & Guests	10

Chairman's Message (continued from left)

that that IEEE-SCV-CPMT chapter is continuing to support the San Jose State University CPMT Student Chapter which is growing and has received financial support from both the IEEE SCV Section and our Chapter. In fact, this year, we are also developing extended collaboration activities with other Universities in the area.

Luu Nguyen of National Semiconductor (now TI) is our chapter's membership upgrade liaison. Luu reminds you that many members are likely eligible to upgrade to senior member. About 9% of the IEEE's membership hold that honorary distinction. The IEEE assigns education credit of 5, 4 and 3 years for PhD, Masters and BA/BS degrees respectively. A total of 10 years education credit + work experience is required for Senior Member Grade.

Contact either Luu Nguyen (l.nguyen@ieee.org) or Ed Aoki (e.aoki@ieee.org) for application details. If you are interested in knowing more about a membership upgrade,

Personal Reflections (continued from left)

engineer. Although I have worked for a number of large firms dominated by electrical engineers, my bachelors degree is in General Engineering.

Career Development

I joined IEEE while I worked at Motorola GEG in the 1980s (after working at Lockheed). My engineering colleagues at Motorola were, by an overwhelming majority, electrical engineers. My motivation was driven my several self-perceptions. These included a sense of awe of the advances underway in electronics and, admittedly, a personal sense of inadequacy.

As I received IEEE literature, I became engrossed in the CPMT Transactions. CPMT was the society in IEEE that most embraced mechanical aspects, and this was a time

Continues in [Reflections](#) page 5

From the Editor's Console

By Joseph Fjelstad

Welcome the latest edition of the CPMT Santa Clara Valley Chapter newsletter. The writers and editors want to thank you the reader for your interest and comments as we continue our efforts to provide you with a useful resource for information on the activities, workings and opportunities related to both your chapter and the IEEE. While we hold to our desire to minimally impact the environment, this newsletter is a special edition and is being printed for distribution at some upcoming events. We will however, continue to be available primarily in digital format through email distribution and though a hyperlink at the Chapter Web Page (www.cpmnt.org/scv). Questions can be directed to Com Chair, Paul Wesling at p.wesling@ieee.org.

We want to continue to emphasize that this is your newsletter and while we intend to provide you with content that we believe is important, we are open to your thoughts about new content and are eager to hear from those with interest in contributing news and information that is relevant to CPMT members. *This month we have two special features prepared by CMPT Excom member and industry analyst Sandra Winkler and reliability expert and former chapter chairman, Dr. Dan Donahoe.*

Please feel free to contact any of us in the Santa Clara Valley chapter with your ideas for content, any contributed materials or your criticism. Thank you again for your membership and interest in the CPMT and if you are not yet a member, I encourage you to join and take advantage of the many benefits the society offers

IEEE – CPMT

Santa Clara Valley Chapter

The leading international society for scientists and engineers engaged in the research, design and development of both evolutionary and revolutionary advances in electronic microsystems including their manufacture, packaging and test.

Chapter Officers

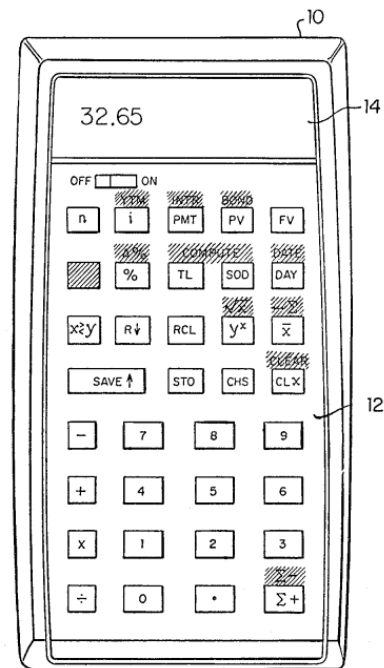
Chairman:	Mudasir Ahmad
Vice chairman:	Ed Aoki
Secretary	Liz Logan
Treasurer	Azmat Malik
Lunch program chairpersons:	Sandra Winkler, Tom Tarter
Dinner program chairman	Harvey Miller, Azmat Malik
Membership chairman	Janis Karklins
Webmaster/Training/Comm	Paul Wesling

E-Mail: cpmt@ieee.org

Electronic Packaging in Santa Clara Valley

The previous parts of this series mentioned the pioneering efforts IC packaging developments of early industry innovators including the invention of the DIP Don Forbes, Rex Rice, and Bryant ("Buck") Rogers also at Fairchild and the development of TAB technology by Frances Hugle at her firm.

Actually IC packaging was a strong hold of technology for the valley for many of the early years. During the 1970s and ramp up of the semiconductor industry to serve the needs of the consumer, there were many interesting innovations that were enabled by IS packaging technology and miniaturization such as the handheld calculator revolution that was lead by HP. Below is the single patent illustration from HP's US Patent No. 3,955,074 titled: "General purpose calculator having keys with more than one function assigned thereto" and awarded to inventors France Rode, William Crowley and Alexander Walker.



Few things in the electronics industry are as iconic as Hewlett Packard's first handheld calculator. The design was classic and nearly 40 years later current versions look very much like the original. Much like the classic VW bug design, some things just work.

Note: if the reader has ideas or suggestions for this series please contact the editor.

MICROMOUSE BEST PACKAGING COMPETITION

2011 IEEE Region-6 & CPMT-SCV Chapter results

by Oscar MahinFallah

The 2011 IEEE Region-6 MicroMouse Competition was held on April 23rd at University of Nevada-Reno, NV. This year, 10 MicroMouse teams competed from University of Hawaii-Manoa; Chico State University, Santa Clara University, DeVry University-Fremont, and University of Nevada-Reno.

The competition encourages college students to learn about robotics, software design & coding, mechanical design, control theory, and system & device packaging design. The “mice” are autonomous electromechanical machines which learn and optimize the solution to a maze. The IEEE Region-6 Central Area presented the cash awards of \$750, \$500, and \$250 to the top three finishers.

This year’s top three finishers based on best time were in order: UNR, UHM, and Chico State. The winning team was Alexandr Bajenov and Erik Chalko for their entry “Nevada Blue”. Kelson Lau, Geoffrey Tran, and Todd Yamakawa, entered their device “FreshmanFTW” (“freshman for the win”) came in second and Chico State’s team “Sam and Company lead by Samuel Mish came in with the third best time. Pictures of the winners are provided here.

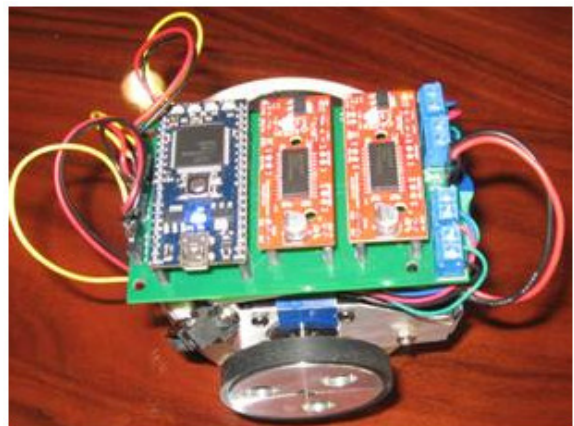


Top maze solver & Best Packaging “Nevada Blue”

An additional prize was awarded by the Santa Clara Valley Chapter of the IEEE- CPMT Chapter for best overall packaging design. To win this award, entries must finish the maze but time is not the determining factor. This award is given based on the following criteria: the solution’s volume, weight, energy storage and consumption, thermal management (for reliability and safety), EMI and noise level. “Nevada Blue” garnered this year’s packaging award in addition to best time and picked up another \$500 for the home team.



Second quickest maze solver: “FreshmanFTW”



Third-place maze solver: “Sam and Company”

Please click on this [short film](#) link to see a video of the competition which captures the maze runs of the winning entries, some bloopers and the awards ceremony for best maze time and best packaging design.

Acknowledgments

The IEEE Region-6 Central Area Chair, Ram Sivaraman, and Oscar MahinFallah of CPMT Santa Clara Valley chapter served as judges for this year’s competition. Special thanks to Dr. Mehdi Etezadi-Amoli, Professor & Chair, Electrical and Biomedical Engineering, University of Nevada, Reno for his efforts coordinating this year’s successful event at UNR. Special thanks also extended to Mr. Ed Aoki and Mr. Allen Earman of IEEE-CPMT for their guidance and coordination of the judging for the packaging contest and to Dr. Mostafa Mortezaie, R6-Central Area Student Activities Chair, for his advisory role to the student branches taking part in the competition

ECTC and the Future of Engineering

By Sandra Winkler, Senior Industry Analyst, New Venture Research (newventureresearch.com)

At the first SVEC (Silicon Valley Engineering Council) banquet I attended, I was quite impressed with the speeches given by the inductees into the Engineering Hall of Fame. Stanley Myers, President and CEO of Semiconductor Equipment and Materials International (SEMI®), spoke of inspiring change, of wanting to encourage young people to create the future. He spoke of the importance of engineering here in Silicon Valley and its effect on the rest of the world. So many of the innovations now in use across the globe were rooted here, in Silicon Valley, and, he added, “What happens here goes around the world in a blink of an eye.”

He alluded to the need for more education in engineering, and a political landscape in which companies can come to Silicon Valley and build on the legacy created by the engineers who turned this valley into what it is today.

What is also needed is a chance for engineers to showcase their research, so that technology can be built upon it. Much of this occurs at the annual ECTC (Electronic Components Technology Conference) event, the premier engineering conference.

The 61st ECTC was held in Lake Buena Vista, Florida, from May 31st through June 3rd, 2011. ECTC features six tracks of papers being presented simultaneously each day for three days, seven papers in the morning and another seven in the evening. Paper topics this year included:

- Advanced IC packaging
- Interconnection
- Optoelectronics
- Materials and processing
- Electronic components and RF
- Modeling and simulation
- Emerging technologies
- Applied reliability
- Assembly and manufacturing technology

There were plenty of papers presented on through-silicon via (TSV) technology, with a focus on palladium-coated copper wire bonds on Friday.

On Tuesday, its opening day, the conference offered an evening plenary session, panel session, seminar, poster exhibits, 61 technology exhibits, luncheon speakers, and a full day of 16 professional development courses to pick from. And of course there was the required evening gala reception for all attendees and their guests. With over 1,000 attendees at the conference,

Continued from left

this year, there was plenty of socializing going on. The May 31st Tuesday night panel session was titled “Spotlight on China.” The Wednesday plenary session was titled “Power Efficiency Challenges and Solutions: From Outer Space to Inside the Human Body,” and the Thursday seminar was titled “Printed Devices and Large-Area Interconnect Technologies for New Electronics.”

I found the Wednesday plenary session the most interesting. Raj Master of Microsoft gave some scary examples of the harm that can come to humans if electronic devices they are holding and operating overheat. Whereas miniaturization, flexibility, and portability are desired traits in consumer electronics, these features also cause overheating, which can lead to product failure and human catastrophes. 3-D packaging doubles the heat density, which degrades product performance by 30 percent. Power and noise both increase, which is why it is important for thermal and noise management to be part of the initial product design.

Sayfe Kiaei of Arizona State University presented a number of forward-looking medical electronics products designed to improve the lives of the disabled. A wireless, swallowable capsule can be used to record data that can then be transmitted to the patient’s doctor. An implantable RF transceiver can be used to treat heart conditions and manage pain, and as an implantable wireless device to act as both sensor and control. The sensor can be used to control prosthetic limbs, powered by RF from outside the body. The RF power could be stored in a transceiver, which gives information to a receiver at the end of the prosthetic or in a pocket. A cochlear implant (in the ear) can be used as a sensor for a prosthetic arm or hand. An integrated hearing aid can have a microphone array to focus which sound to pay attention to; a MEMS device can be used for this with its small size. An adapted microphone can cancel background noise.

There were more technology exhibits this year in Florida than ever before. ITRI’s John Lau was showing off some interesting new 3-D technology, which starts with a 5- μm wafer. This is thin enough that one could see through it when holding it up toward the ceiling facing the light!

Next year’s ECTC event will be held in San Diego, California, May 29 through June 1st, 2012. See you there!

Contact Sandra at
slwinkler@newventureresearch.com)

Personal Reflections (continued from page 1)

in which technical change was largely driven by innovation of electrical components and integration of electronics into products. Reading the CPMT Transactions drove me to the ASU library to read further on many subjects, primarily materials science (a course not in my undergraduate curriculum).

I worked for a couple additional defense electronics firms (Ford Aerospace and Teledyne), but my deeper involvement in IEEE developed after the end of the Cold War. After the Berlin Wall fell, I transitioned to commercial electronics with Compaq Computer. Compaq was a company growing so fast that President Reagan had visited to see who was affecting the international balance of trade. As a consequence of explosive growth, the Compaq working environment offered challenges.

At Compaq, I used what I saw as the congruence of my skills with apparent needs. Commercial electronics did not embrace the level of rigor common in military electronics, and I saw an opportunity to contribute in a meaningful way. Eventually, my small group was moved to reliability engineering. I sought out help after that organization shuffle, again, using IEEE connections. Mike Pecht at the University of Maryland (IEEE Fellow) and his staff offered much assistance. He invited me to participate in an IEEE reliability standard. Through this activity, I learned much about standards activities, and I have since participated in a number of standards in other standards bodies.

While at Compaq, I began to serve as an Associate Editor of the CPMT Transactions under Avi Bar-Cohen. Avi spent a good deal of time training me how to be an editor. My writing skills definitely improved.

After ten years at Compaq, I moved to a disk drive company for a year. I then worked for Mike Pecht in his reliability lab for two years. This was a life changing experience, because the University had such a rich collection of equipment and so many expert faculty and staff. ON a part time basis, I complete a dissertation on a reliability aspect of ceramic capacitors. Since 2006, the University has monitored how many times each dissertation has been downloaded. At this time, that download number is approximately 3000 times. If it had not been for IEEE, I probably would not have had this opportunity.

I took a job in Menlo Park with a consulting firm after the two years at the University of Maryland. I became active in IEEE in Santa Clara Valley in the hope of finding consulting work. Although I did find some consulting work, what I found in IEEE/SCV was a group of volunteers in the finest traditions of professionalism. Paul Wesling (Fellow IEEE) provided me with a complete set of the IEEE/SCV newsletter called “Grid”

Personal Reflections (continued from left)

going back to its beginning. I used this to write a short chapter history for Allen Earman’s CPMT/SCV chapter guideline. As I read through the decades of Grids (during which Silicon Valley was created), I enjoyed reading between the lines of history. For example, student protests at the University of Illinois in Champaign-Urbana drove the first big parallel process based mainframe to government facilities in the Bay Area. The consequential software job listings were clearly listed in “Grid”.

Paul Wesling continues with an electronic version of Grid he calls eGrid. This is a one page summary of technical talks in the valley. There are typically more than one each weekday. For the most part, these talks are free to the public. For the most part, these talks are riveting, because these talks are provided by the people who are actually doing the work they are discussion. All the drama of real life people is evident.

During my period in Menlo Park, I volunteered to give some presentations for CPMT/SCV. Harvey Miller, a Silicon Valley icon, has long served as the organizer of the CPMT presentations. My first presentation was on economics and engineering for a joint meeting of GOLD and CPMT. In doing this presentation, I invited a colleague from the east coast who had an economics undergraduate degree. She and I have since coauthored several presentations and articles.

I served as Secretary, Chair and Vice Chair of CPMT/SCV chapter. The CPMT chapter had a long history, one of the longest in Silicon Valley. Allen Earman (who became the IEEE/SCV section chair) insisted that I participate in the section meetings. Of course Allen was correct. I also found this to be a wonderfully insightful experience, because I was meeting the people who were the backbone of Silicon Valley.

The IEEE connections transcend just one organization. I created the Silicon Valley Engineering Council Journal by requesting articles from my many IEEE colleagues. The Journal has now been in three volumes.

Currently, I am serving on the Board of Governors of CPMT. This is an exciting opportunity, and I hope to bring more technical scope and breadth to CPMT related to the word “components”.

Conclusion

My library research has since grown since the 1980s to become habit. I have held citizen library cards at many local university libraries, and my interests have expanded to allied subjects. My IEEE colleagues have been of great help to me in learning about electronics. I have transitioned from a general engineer to an electronics engineer.

IEEE/SCV is a pot of gold. It is there for you.

IC Packaging Continues to Blossom

By Sandra Winkler, New Venture Research
(newventureresearch.com)

The year 2010 was a banner year for the semiconductor industry, pulling out of the Great Recession of late 2008 to early 2009 much faster than other industries. Handheld gadgets from smart cell phones to tablets are the primary drivers behind this recovery; the auto industry is also on an uptick. A few select end products are listed below:

	2010 Units (M)	2015 Units (M)	CAGR
Notebook PCs	200	300	8.4%
Tablets	12	125	59.8%
Hard disk drives	450.6	645.9	7.5%
CD/DVD Drives	361.3	440.6	4.0%
Flash Drives	400	535	6.0%
Cell phones	1,302	1,954	8.5%
- Smart phones	205	416	15.2%
- Dumb phones	1,097	1,538	7.0%

Tablets are new to the market, thus have low unit figures. However, the compound annual growth rate (CAGR) of 59.8 percent is impressive enough to make one take notice. Smart phones also have an impressive growth rate of 15.2 percent for the years 2011 through 2015. And the hard disk drives, CD/DVD drives, and flash drives are just simply large markets. All of this points to a healthy market for ICs going forward.

The shipment of ICs grew 28.9 percent from 2009 to 2010. The prevalence of ICs in our daily lives, keeping us connected all the time, will continue to show an annual increase, but a slower growth, of 7.52 percent compound annual growth rate (CAGR) from 2010 through 2015. Unit shipments of ICs will be 267,811 million in 2015. Approximately 68 percent of these shipments are leadframe based throughout the forecast period. With this industry having its cycles every four years (a downturn or softening of the market the first year of a new president in the United States), 2013 will see a tapering of growth rates, to only 4.8 percent that year. After a revenue growth of 31.3 percent from 2009 to 2010, the CAGR for IC revenue will be 7.42 percent for the years 2011 through 2015. Revenue for these chips will grow from \$249,911 million in 2010 to \$357,413 million in 2015. This is still quite healthy, although slightly behind unit growth.

IC Packaging Continued from left:

The total revenue for IC package assembly was ~\$38.5B in 2010, which is predicted to expand to \$57.1B by 2015. Package assembly revenue growth will be at an 8.18 percent CAGR through 2015, ever so slightly ahead of the total IC revenue growth of 7.42 percent.

The Role of Packaging

Packaging of these integrated circuits is important, as the package holds the footprint to the PCB, and can either facilitate or hamper the speed and performance of the chip. Attachments to the package such as heatsinks must also dissipate the heat coming from the chip; failure to remove excess heat can cause device failure. Thus the right package, made of the right materials, is critical.

The change in the unit percentages in the IC package mix vary. Array packages, QFNs, and WLPs are on the rise as a percentage, while TSOPs are showing a decline as a percentage. While TSOPs largest market - standard logic - is holding relatively even, the package is losing ground in the large memory market sector.

So what are the largest growth areas for IC packages? Stacked packages and SiPs, which largely are packaged in FBGA solutions, both of which are growing in the vicinity of 16 percent compound annual growth through 2014.

QFNs and Inner-Row QFNs, which allow for a great expanse of I/O counts, which are edging in on territories previously held by SOs and QFPs. QFNs are growing at 10.45 percent CAGR through 2015, while the newly-introduced Inner-Row QFN will grow at a staggering 107 percent through 2014.

Wafer Level Packages (WLPs), which capture the very low end of the market, will broaden its reach with the adoption of Fan-out WLPs. Fan-out WLP have an added overmold which expands beyond the edge of the chip, allowing for a larger surface for electrical traces beyond what is capable with traditional WLPs, which allows for considerably higher I/O counts. WLPs are growing at 13.85 percent CAGR through 2015, while Fan-Out WLPs are growing at 38.4 percent CAGR through 2014.

Flip chip interconnection, which can be incorporated into a variety of package solutions, is growing at a CAGR of 31.3 percent through 2014 for in-package solutions. While PGA, BGA, and FBGA package solutions are obvious selections for a flip chip interconnection style, flip chip can also be utilized on leadframe packages as well, such as the DFN and QFN package solutions. [Continues on Page 8:](#)

Meetings You May Have Missed

The Santa Clara Valley chapter of the IEEE CPMT Society is among the most active in the world and is constantly striving to provide valuable information in a timely manner. Much of the credit for the success of the meetings rests at the feet of our outstanding programming team, co-chairs Azmat Malik and Sandra Winkler assisted by Harvey Miller. Following is a sampling of some of the outstanding presentations to which members have been treated this year. Use links to view files or for more information.

["Developments in MEMS Packaging"](#), Alissa M Fitzgerald, AMFitzgerald and Associates

["Embedded Passives: Packaging Paradigm of the Future?"](#), Jason Ferguson, Crane Naval Surface Warfare Center

["Impact of Packaging on Photovoltaic Panel Performance and Reliability"](#), Alelie Funcell, Renewable Energy Test Center

["Novel Fine Pitch, Low Profile, Low Cost Connector Technology"](#), David Light, VP Technology, Neoconix

Other offerings:

Second Annual ["Soft Error Rate \(SER\) Workshop"](#), Seven 20-minute talks; slides and WebEx viewing; links (3 hour seminar)

["Moore's Law for System Integration"](#), Prof. Rao Tummala, NSF Packaging Research Center, Georgia Tech (2 hour seminar)

["All-Silicon System with Nano-Packaging: Highest Functionality, Lowest Cost, Smallest Size"](#), Prof. Rao Tummala, NSF Packaging Research Center, Georgia Tech

["Design of High Density & 3D Packaging: Tools and Knowledge"](#), Thomas S. Tarter, Package Science Services LLC

Up Coming Meetings

Continuing to provide educational opportunities to its members, your CPMT chapter has lined up an outstanding program with top tier speakers and timely topics for the fall. Below is a sampling of some of what is on tap. Mark the dates!

["Memory Scaling and Its Potential Impact on Computing and Storage"](#) Ed Doller, VP and Chief Memory Systems Architect, Micron Technology -- **lunch** Thursday, September 22

["Silicon Carbide \(SiC\) Sensing Technology for Extreme Harsh Environments"](#) Debbie G. Senesky, Ph.D., University of California, Berkeley -- **dinner** Wednesday, October 12

Other Upcoming Events:

SF-**GOLD+Students** - 8/18 | **Engineers of Tomorrow: Preparing for the Job Market** - challenges, opportunities, getting started, hone your skills, today's competitive job market ... [\[more\]](#)

SFBAC - 8/21 | **IEEE Tour of the Computer History Museum** - optional lunch, "Revolution" exhibits, for whole family ... [\[more\]](#)

SCV-**PACE** - 8/22 | **USA Public Policy: Concerns for Engineers** - 112th Congress, issues affecting IEEE members, science education, start-up companies ... [\[more\]](#)

IEEE Reaches Out to Help Members

In view of the continuing economic turmoil the IEEE, realizing its value of its members is making it possible new or continuing membership during a period of special circumstances which include: unemployment low income, retirement and disability Full details can be found on the web at the link below.

http://www.ieee.org/web/membership/Cost/special_circumstances.html

Want the Latest Schedule of CPMT Events? Seminars and Short-Courses? Check out our Web Page at www.cpmc.org/scv.

For CPMT and all SF Bay Area IEEE Chapter Events go to the eGRID at <http://e-grid.net/>

IC Packaging Continued from page 5:

Stacked packages are a special form of a multi-chip package, one which places the die vertically on top of one another. The stacked package and SiP markets are being driven by the wireless communication and digital data storage markets. High-density memory for data and image storage, as well as higher speeds for read and write, are required to meet the needs of the marketplace. The complexity and number of features in handheld products such as cell phones continue to increase, while pressure for small and lightweight products also persists. Stacked packages are useful in meeting both of these conflicting needs.

Speed, performance, signal integrity, and package density are key drivers of this technology. Many of these devices are placed in portable devices, and increasing the density of the packaged devices can reduce the size of the end products. This both reduces the cost of the final product (system cost), as less material is used, and increases the desirability of the final product in the eyes of the consumer.

Stacked package options include:

Die Stack - die within a single FBGA

Package on Package (PoP)

Package in Package (PiP)

Stacked TSOPs or within a TSOP

Stacked QFN or within a QFN

Stacked MCMs

Stacked WLPs

A full 50% of all stacked packages are die stack packages. This technology keeps all the die stacked on a single substrate. PoP solutions comprise 36 percent. The PoP solution mixes technologies, such as memory and logic. This allows for each of the device types to be tested separately then assembled. Both die stacks and PoP solutions will likely be reduced as a percentage of the total over time, as PiP, stacked QFN, and WLPs gain ground. PiPs also allow for dissimilar technologies, but with the top device inverted or upside down and all devices on a common substrate and overmold. Roughly 75 percent of stacked packages find use in phones.

System in package (SiP)

System in package (SiP) is a customized package with multiple elements inside, in a standard JEDEC footprint. A SiP can be one or more semiconductor die and passives (resistors and/or capacitors), or two or more chips that form a system, such as a processor plus memory, integrated into a single packaged unit. Die embedded within the substrate with other devices

IC Packaging Continued from left:

on top of the substrate qualify. However, one die plus a decoupling capacitor does not qualify. A SiP can be thought of as a functional block. It operates as a system to achieve a level of performance beyond what can be accomplished by placing the components into individual packages. Like an MCM, because more activity is happening within the package, fewer leads are required in and out of the package in relation to other large and complex devices.

The die within a SiP can either be placed next to each other horizontally or stacked vertically, blurring the definition between stacked packages and SiPs. When a stacked package contains enough elements to be a system, then it is placed in this category.

A SiP attempts to fill the need for a semi-custom package with not-so-exotic parts, thus differentiating it from the more complex and customized MCM. The goal is to create a packaged part that costs less than an MCM and can fit into a greater number of everyday end products. An individual SiP should be easily modifiable so as to go into different products than the one for which it was originally created, and have some degree of scalability to upgrade the device.

A common package platform such as a BGA, with a JEDEC footprint, would also distinguish a SiP from the more customized MCM. A standard package format also makes the part transparent to the user for ease of assembly.

The end result of both a SiP and an MCM is that the individual pieces of a unit are in close proximity, thus can operate at higher speeds and with lower power consumption than if the individual pieces were farther apart in separate packages. The number of I/Os on the package is reduced in comparison to separately packaged parts, due to the functional block nature of the package, in which many functions are being handled within the package with fewer connections needed outside the package. If discrete devices are incorporated within the SiP, then these do not require tracing on the PCB. In addition, less space is consumed on the PCB, allowing for shrinkage of the final product. Any number of end applications can benefit from these dynamics. Certain medical devices, such as hearing aids, and cameras that are swallowed to provide images of the intestinal tract, require this small form factor. Any handheld, battery-operated device, such as a cellular telephone, can benefit.

Cell phones again are the largest market for SiPs, with approximately 69 percent of all SiPs going into these products. Another 10 percent will be captured to the base stations that serve the cell phones.

Continued on page 9:

IC Packaging Continued from page 8:

QFNs and Staggered Inner-Row QFNs

QFN, or quad flat pack no-lead, packages are a more recent package introduction than the more established packages such as the SO, but they have quickly attained popularity. The QFN is in the chip scale package (CSP) category, being close to die sized. It has leads on four sides of the package, which are encapsulated within the mold compound so that the package rides flat on the printed circuit board (PCB). The lack of visible leads protruding from the bottom gives this package the name “no lead.”

The shortened lead length increases the speed of devices, as the electron does not travel quite as far to reach the PCB from the die. The entire leadframe is reduced in size due to the closely cropped nature of the package in relation to the die, and to the shortened lead length, which does not have the external gullwing leads.

The QFN offers thermal performance superior to that of leaded packages of similar body size and I/O count. The leadframe is on the bottom of the package; thus the die attach pad is exposed, allowing it to be easily soldered directly to the board, and allowing heat to dissipate into the PCB. Heat transfers faster into solid material than into ambient.

QFNs currently house a large number of devices; the largest markets include 8-bit MCUs, standard logic, voltage regulators and references, and both special purpose logic and analog communications chips.

Extending the Lead Count

To further increase the reach of this package, the latest development in QFN packages is to extend the number of rows of leads from the usual one to two or three rows of leads. The leadframe is stamped or etched as in any other leadframe solution, but the leads are of various lengths, either two or three different lengths. When bent downward for connection to the PCB by trim and form equipment, the result is a staggered-row, array-patterned package solution, with a hole in the center. This allows the number of package leads to extend into the hundreds, up from generally fewer than 50 with a traditional QFN. The resulting package is a high-density, leadframe array package. The staggered inner-lead QFN has the ability to capture the lower-end of the QFP (quad flat pack) market. This includes extending its reach to higher-bit MCUs and both logic and analog communications chips, largely bound for handheld gadgets that require a small form factor package.

Wafer Level Packages (WLP) and Fan Out Overmolded WLPs Wafer-level packages (WLPs) are formed on the die while they are still on the uncut wafer. The process can

IC Packaging Continued from left:

be thought of as an extension of front-end manufacturing in that it involves the entire wafer, but is more similar to bumping for flip chip and TAB operations. The result is that the final packaged product is the same size as the die itself. Singulation of the device occurs after the device is fully packaged, unlike traditional forms of packaging.

Most WLP designs place the active circuits face down for the shortest electrical path. The active circuits can also be face up, with electrical connections either through the silicon or wrapping around the silicon. Through-silicon designs allow for wafer stacking, such as in the Tru-Si model. Face-up WLPs can be used for signal-sensitive devices and fine-pitch interconnections as well.

Fan Out Overmolded WLPs

Reconfigured or fan-out overmold wafer-level packages were introduced in 2006. After devices are manufactured on a wafer, the devices are sawn and transferred on a carrier to another larger wafer that has gaps between die, which are filled with overmold material that also coats the back side of the devices for protection. This allows for a larger surface on which to extend a redistribution layer, thus allowing for far more I/Os than would be possible on the original smaller surface. Solder balls or bumps can be added to this surface for interconnection to a printed circuit board.

The WLP Market

While WLPs are used for logic, memory, and analog devices, it is the analog market that is the largest for WLPs. Voltage regulators and references, found in all electronics, are a large market for WLPs. WLPs are quite suitable for these devices, as WLPs are traditionally a low-I/O package, which match the I/O demand of voltage regulators and references.

Fan-Out Overmolded WLPs extend the I/O count beyond just the number of I/O which can fit on the face of a small IC. Fan-out overmold WLPs are utilized to package baseband processors, RF and analog, power management, and analog and logic ASICs, including application processors, power amplifiers, and within MCMs to create a radio-in-package (RiP) device. More applications will be found for these packages subsequently.

Flip Chip Interconnection

Flip chip interconnection places the die is flipped face

[Continues on next page:](#)

IC Packaging Continued from page 9:

down (or active side down) so that the circuitry faces the substrate. Unlike wire bonding, in which the connections are made at the periphery, flip chip connections are in an area array covering all or part of the face of the die. Flip chip is almost always performed on packages with substrates, although a few designs utilize leadframes. The die does not have to be face down with leadframe designs; the leadframe can be designed to reach over the top of the die in a face-up position for interconnection, as is the case with Carsem's FCOL. This maintains the face-up position away from the PCB, preventing cross talk with the PCB, which is important with RF chips. The electrical connection is made through bumps on the face of the die, which then connect directly to the substrate below. The bumps are in an array pattern on the face of the die, and are placed on the surface of the die while the die are still on the uncut wafer. Individual die can also be bumped, but this is not a cost-effective solution.

The processes involved with flip chip technology tend to be expensive and sometimes difficult, although less expensive than wire bonding when I/O numbers are high. Flip chip is not suitable for every application, and tends to be used for high-performance, high-I/O devices, and low-I/O devices in space-constrained areas. Flip chip allows for a higher density of interconnection points than does wire bonding, as the array pattern of bumps on the die surface allows for a greater percentage of the total device surface to be used for interconnect. This is in contrast to just the periphery being used, as in the case of wire bonding. Because the interconnection to the substrate is made beneath the die, not out to the periphery of the die as in wire bonding, a smaller form factor is achieved in the overall package size; hence the use of this technology in space-constrained areas. Given the shortened electrical distance to the board, flip chip also offers greater speed with less parasitics.

The use of flip chip becomes mandatory on any die with an I/O count so high that the pads cannot fit around the die perimeter. Though this number is die specific, it almost certainly applies at I/O counts above 700. Due to the shorter length in the interconnection, flip chip also has lower signal transmission losses in relation to wire bonding. High clock speeds and increasing functionality of the chip drive the need for higher I/O counts and faster package performance than is obtained through the use of wire bonding. Most microprocessors switch to flip chip when their clock speeds reach 400 MHz. Flip chip is also used for some high-frequency RF devices. Flip chip is used for a number of applications,

IC Packaging Continued from left:

including computers and game consoles, networks and communications, and mobile platforms. Frequency, battery life, and miniaturization are all issues for mobile applications. Typical devices utilizing flip chip include chips at the high end such as MPUs, graphics chips, field programmable gate arrays (FPGAs), and programmable logic devices (PLDs). Flip chip also has a niche at the bottom of the market, with low I/Os in space constrained products. Devices with flip chip with low I/O generally do not require underfill beneath the die to accommodate the CTE mismatch, although it is often used on handheld devices anyways to assist with the "oops" factor.

Smaller, Faster, Cheaper - still the Theme

The fastest growing packages and technologies are well suited for space-constrained locations, and will find themselves in handheld items purchased by average consumers. Long gone are the days when military and space applications dominated the demand for ICs - individual consumers now control much of the market. Consumer items costing \$400 and under still sold well during the Great Recession. Demand for cell phones, particularly smart phones, tablets, digital cameras, automobiles laden with ICs, and more will continue to keep demand for ICs on an upward trend.

Whizz Systems Open House for IEEE & Guests



Pictured are some of crowd who came to Whizz Systems recent open house. Participants were treated to information packed tours of the company's Santa Clara Valley operations which include an SMT manufacturing plant and engineering design support center.

The Santa Clara Valley CPMT chapter salutes and extends thanks to Whizz Systems for its outstanding educational support efforts.