IEEE Heterogeneous Integration Roadmap Symposium

Hosted by IEEE Electronics Packaging Society Santa Clara Valley Chapter

Thursday, February 22nd, 2018
8:30 AM to 6:00 PM
at
Texas Instruments Building E Conference Center,
Silicon Valley, California

Roadmap Symposium Web Link
http://www.cpmt.org/scv/?p=513

Jointly Sponsored by

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Register at 1802symp-eps.eventbrite.com

Date
Thursday, February 22nd, 2018
8:30 am to 6:00 pm

Attendee Registration Fee
$40 IEEE members, students, retired, unemployed,
$50 non-members
Add $10 more after Feb. 9th

Location Texas Instruments Auditorium
Building E Conference Center,
2900 Semiconductor Drive,
Santa Clara, California, USA

Silicon Valley Companies that have already registered
Intel, Google, Xilinx, Cisco, Nvidia, Texas Instruments, Analog Devices

HETEROGENEOUS INTEGRATION ROADMAP

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IEEE HIR ROADMAP MORNING Program Feb 22, 2018

8:30 – 9:00 am **REGISTRATION**
9:00 – 9:15 am **SYMPOSIUM OPENING** ***William Chen*** *(HIR)*
Jonathan Davis, Nicky Lu, Rolf Aschenbrenner, *(USA, Asia, Europe)*

Session 1 –Chaired by ***Samar Saha*** *(IEEE Electronics Devices Society)*

9:15 – 10:50am **Heterogeneous Integration for High Performance**

- 9:15-9:30am High Performance Computing & Data Center **Kanad Ghose** (Binghamton U)
- 9:30-9:45am Co-Design **Andrew Kahng** (UCSD)
- 9:45-10:00am 3D +2.5D Ravi.Mahajan (Intel), **Raja Swaminathan** (Intel)
- 10:00-10:15am WLP (fan in and fan out) **Rozalia Beica** (DOW), John Hunt (ASE)
- 10:15-10:30am Integrated Photonics **Amr Helmy** (U Toronto) Bill Bottoms (3MTS)
- 10:30-10:45am Test **Dave Armstrong** (Advantest)
- 10:45-10:50am Q&A

BREAK

Session 2 –Chaired by ***Bill Bottoms*** *(IEEE Electronics Packaging Society)*

11:05 – 12:40pm **Heterogeneous Integration for Consumer & Industrial Applications**

- 11:05-11:20am Medical and Health & Wearable Mark Poliks (Binghamton U) Nancy Stofell (GE)
- 11:20-11:35am SiP & Module **Rolf Aschenbrenner** (Fraunhofer IZM), Klaus Pressel (Infineon)
- 11:35-11:50am Single Chip and Multi Chip Packaging **William Chen** (ASE), Annette Teng (Promex)
- 11:50-12:05pm Integrated Power Package **Doug Hopkins** (NCSU), Louis Burgyan (LTEC)
- 12:05-12:20pm Emerging Devices **Myya Meyyappan** (NASA Ames)
- 12:20-12:35pm IoT **Robert Lo** (ITRI Taiwan)
- 12:35-12:40pm Q&A

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IEEE HIR ROADMAP AFTERNOON Program Feb 22, 2018

12:40 – 1:40pm **LUNCH**
1:40 – 2:25pm **PLENARY PRESENTATION Dr. Nicky Lu** (Etron)
"Synergistic Growth of AI and Silicon Age 4.0 through Heterogeneous Integration of Technologies"

Session 3 –Chaired by **Luu Nguyen** (IEEE Electronics Packaging Society)

2:25 – 3:45pm **Heterogeneous Integration for Special Applications**

- 2:25-2:40pm Aerospace & Defense **Tim Lee** (Boeing), Daniel Green (Darpa)
- 2:40-2:55pm 5G in RF and Analog Mixed Signal **Tim Lee** (Boeing), Herbert Bennett (AltaTech Strategies LLC)
- 2:55-3:10pm Interconnect **Subramanian Iyer** (UCLA)
- 3:10-3:25pm MEMS & Sensor integration **Shafi Saiyed** (ADI)
- 3:25-3:40pm Cyber Security **Sohrab Aftabjahani** (Intel), Scott List (SRC)
- 3:40-3:45pm Q&A

BREAK

Session 4 –Chaired by **Subramanian Iyer** (IEEE Electron Devices Society)

4:00 – 5:20pm **Heterogeneous Integration Applications, Materials & Simulation**

- 4:00-4:15pm Mobile **William Chen** (ASE)
- 4:15-4:30pm Automotive **Venky Sundaram** (GT), Rao Tummala (GT)
- 4:30-4:45pm Simulation **Christopher Bailey** (Greenwich U), Xuejan Fan (Lamar)
- 4:45-5:00pm Materials & Emerging Research Materials **Bill Bottoms**(3MTS), MJ Yim (Intel)
- 5:00-5:15pm Supply Chain **Tom Salmon** (SEMI)
- 5:15-5:20pm Q&A

5:20 – 5:45pm **WRAP UP** ***William Chen, Bill Bottoms*** (HIR)
5:45 – 6:00pm **SYMPOSIUM CLOSING** ***Dr. Gaurang Choksi*** (Intel)

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Feb 22nd 2018 Plenary Talk

"Synergistic Growth of AI and Silicon Age 4.0 through Heterogeneous Integration of Technologies"

Dr. Nicky Lu

CTO and Founding Chairman, Etron Technology, Inc.
Executive Director, Taiwan Semiconductor Industry Association, Taiwan

CEO and Founding Chair of Etron Technology, Inc. since 1991, and co-founded several successful IC companies including Ardentec and Global Unichip. He received his B.S. in Electrical Engineering from National Taiwan University and M.S. and Ph.D. from Stanford University. He worked for IBM and won numerous IBM recognition awards including an IBM Corporate Award. He holds over 27 U.S. patents and published over 50 technical papers. He received an IEEE Solid-State Circuits Field Award for his contributions in high speed DRAM cell/array technologies and chip designs. Dr. Lu is an IEEE Fellow, a Member of the National Academy of Engineering of U.S.A.

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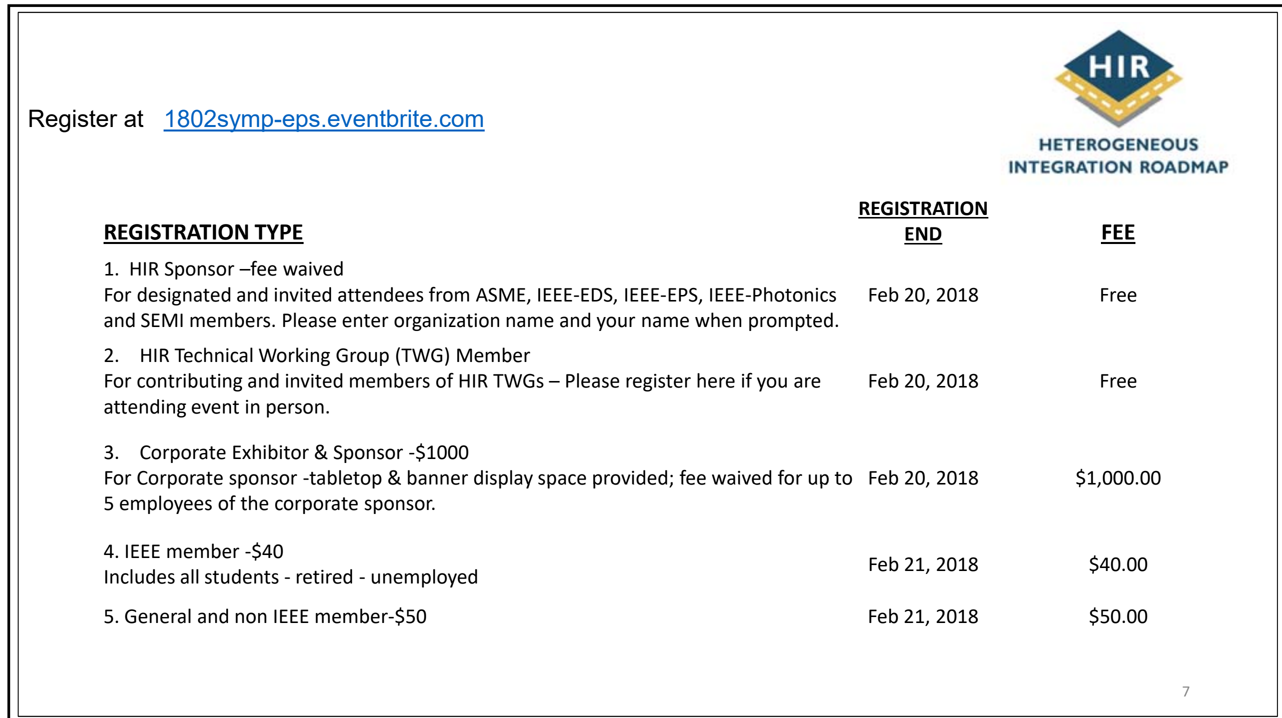
Feb 22nd 2018 Closing Remarks

Dr. Gaurang N. Choksi

Vice President, Technology and Manufacturing Group
Director, Assembly and Test Technology Development Core Competencies

Dr. Choksi joined Intel in 1988 to work on semiconductor packaging for the Intel 386 processor family of products. During his tenure at Intel, he has contributed to a variety of areas, including mechanical analysis and testing, multi-chip module design and analysis, and design tool development for packages and boards. He has worked in the areas of electrical and mechanical analysis tool development and deployment as well as package- and board-level CAD tools and integrated circuit package co-design. He has also managed the package design and analysis teams. He has numerous publications in the fields of fracture mechanics, finite element analysis, composite materials, and design and design tools for electronic packaging. He won an Intel Achievement Award for electronic package design and analysis software development. Dr. Choksi earned a B.S. in mechanical engineering from the University of Madras, India, and received his Ph.D. in engineering science and mechanics from Virginia Tech.



Register at 1802symp-eps.eventbrite.com

HIR
HETEROGENEOUS INTEGRATION ROADMAP

REGISTRATION TYPE	REGISTRATION END	FEE
1. HIR Sponsor –fee waived For designated and invited attendees from ASME, IEEE-EDS, IEEE-EPS, IEEE-Photonics and SEMI members. Please enter organization name and your name when prompted.	Feb 20, 2018	Free
2. HIR Technical Working Group (TWG) Member For contributing and invited members of HIR TWGs – Please register here if you are attending event in person.	Feb 20, 2018	Free
3. Corporate Exhibitor & Sponsor -$1000 For Corporate sponsor -tabletop & banner display space provided; fee waived for up to 5 employees of the corporate sponsor.	Feb 20, 2018	$1,000.00
4. IEEE member -$40 Includes all students - retired - unemployed	Feb 21, 2018	$40.00
5. General and non IEEE member-$50	Feb 21, 2018	$50.00

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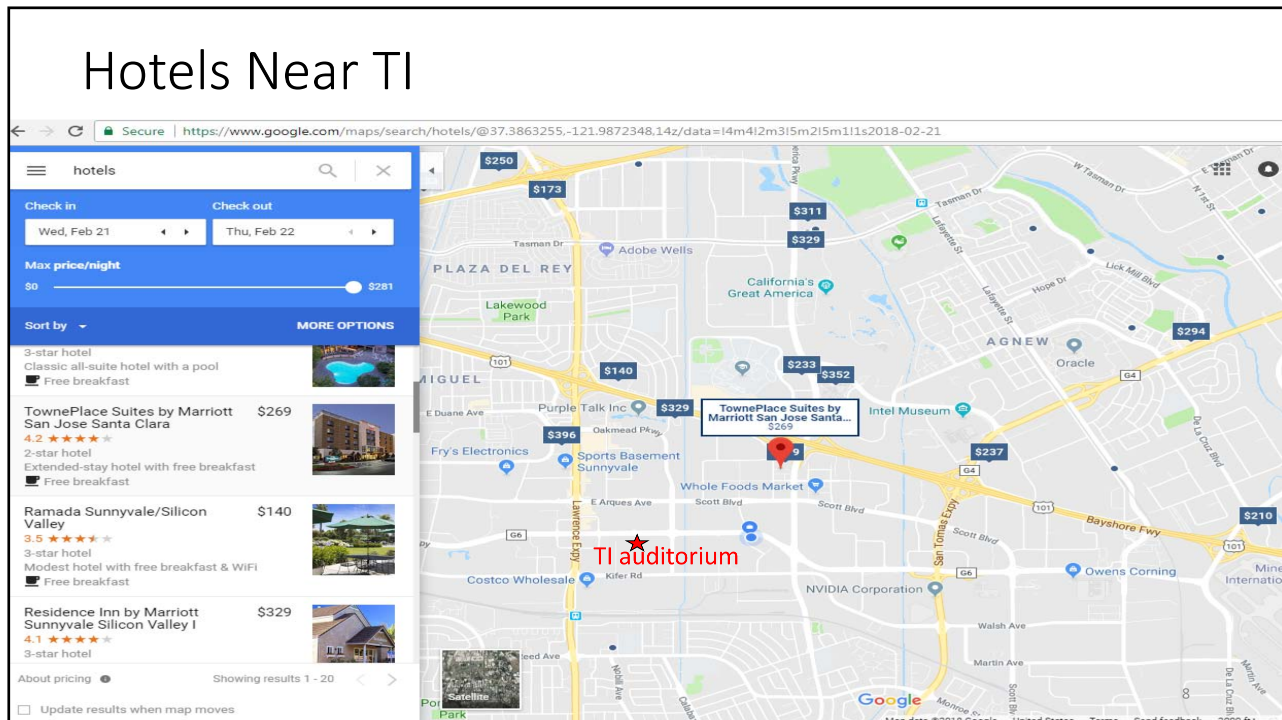

Some Hotels Nearby

Ramada Inn www.ramada.com
1217 Wildwood Ave, Sunnyvale, CA 94089
408-245-5330

Avatar Hotel (next to IHOP) jdvhotels.com/avatar
4200 Great America Pkwy, Santa Clara, CA 95054
408-235-8900

Embassy Suites by Hilton embassysuites3.Hilton.com
2885 Lakeside Dr., Santa Clara, CA 95054
408-496-6400

Tips for travelling to Silicon Valley.

1. Book your hotels early as rooms usually fill up on weekdays.
2. Road Congestion times: 7:00-10:00am & 2:30-7:30pm
3. Lyft and Uber are very convenient to get around in Silicon Valley
4. Fly into San Jose Airport, California (SJC); minutes from TI venue
   Not to be confused with San Jose Airport, Costa Rica (SJO)

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