2nd Annual

Heterogeneous Integration Roadmap 2-Day Symposium

Hosted by SEMI International and **IEEE-SCV Electronics Packaging Society**

Thursday & Friday, 21-22 February 2019

at

SEMI Global Headquarters
Silicon Valley, California

Thursday, 21 February – 8:30 AM – 6:00 PM (PT)
Friday, 22 February – 8:30 AM – 4:00 PM (PT)
Attend both days, or either day (same low fee)

Visit: http://www.cpmt.org/scv/?p=513

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Dates
Thursday, February 21st, 2019: **Introduction to HIR v1.0**
8:30 AM to 6:00 PM (PT)

Friday, February 22, 2019: **TWG*** **Sessions for HIR v2.0**
(HIR TWG Caucus & Cross-TWG Meetings)
8:30 AM to 4:00 PM (PT)

HETEROGENEOUS INTEGRATION ROADMAP

Attendee Registration Fee *Add $10 after Feb. 8th*
$40 – non-members
$25 – IEEE/ASME members, SEMI company employees
$25 – Students, retired, unemployed
(Registration includes refreshment breaks and box lunch both days)

Location SEMI Global Headquarters
673 South Milpitas Blvd
Milpitas CA 95035 USA

* **TWG** = **T**echnical **W**orking **G**roup

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IEEE HIR ROADMAP MORNING Program Thursday 21 February 2019

8:30 – 9:00 AM **REGISTRATION**
9:00 – 9:15 AM **SYMPOSIUM OPENING** **William Chen** (HIR co-chair)
Greetings from Representatives from USA, Asia, Europe

Session 1 – Chair TBD
9:15 – 10:50 AM **Heterogeneous Integration for High Performance**
- **High Performance Computing & Data Center**, Kanad Ghose (Binghamton U), Dale Becker (IBM)
- **3D and Interconnect**, Ravi Mahajan (Intel)
- **WLP (fan-in and fan-out)**, Rozalia Beica (DOW), John Hunt (ASE)
- **Thermal Management**, Madhu Iyenger (Google), Azmat Malik
- **Integrated Photonics**, Amr Helmy (U-Toronto), Bill Bottoms (3MTS)
- **Test**, Dave Armstrong (Advantest)
- Q&A

BREAK

Session 2 – Chair TBD
11:05 – 12:40 PM **Heterogeneous Integration for Consumer and Industrial Applications**
- **Emerging Devices**, Meyya Meyyappan (NASA Ames)
- **Medical, Health and Wearables**, Mark Poliks (Binghamton U), Nancy Stoffel (GE)
- **SiP & Modules**, Rolf Aschenbrenner (Fraunhofer IZM), Klaus Pressel (Infineon)
- **Single Chip and Multi Chip Packaging**, William Chen (ASE), Annette Teng (Promex)
- **Integrated Power Packaging**, Doug Hopkins (NCSU), Patrick McClusky (UMD)
- **IoT**, Robert Lo (ITRI Taiwan)
- Q&A

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IEEE HIR ROADMAP AFTERNOON Program Feb 21, 2019

12:40 – 1:20 PM **LUNCH** (discussions; box lunch included)
1:20 – 2:00 PM **PLENARY PRESENTATION**
Invited Speaker: Babak Sabi, Corporate Vice President, General Manager of Assembly & Test Development, Intel Corporation

Session 3 – Chair TBD
2:05 – 3:45 PM **Heterogeneous Integration for Special Applications**
- **Aerospace and Defense**, Tim Lee (Boeing)
- **5G in RF and Analog Mixed Signal**, Tim Lee (Boeing), Herbert Bennett (Alta Tech)
- **Cyber Security**, Sohrab Aftabjahani (Intel)
- **Simulation**, Chris Bailey, (U-Greenwich), Xuejun Fan (Lamar)
- **MEMS and Sensor Integration**, Shafi Saiyed (ADI)
- Q&A

BREAK

Session 4 – Chair TBD4:00 – 5:20pm **Heterogeneous Integration Applications, Materials & Simulation**
- **Automotive**, Urmi Ray (SCI-GTS), Rich Rice (ASE-US)
- **Mobile**, William Chen (ASE)4:30-4:45pm **Co-Design**, TBD
- **Co-Design**
- **Materials and Emerging Research Materials**, Bill Bottoms (3MTS)
- **Supply Chain**, Tom Salmon (SEMI)
- Q&A

5:20 – 5:45pm WRAP UP; Next Day's Plans – William Chen, Bill Bottoms (HIR co-chairs)
5:45 – 6:00pm SYMPOSIUM CLOSING

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Symposium Co-Hosted by IEEE-EPS Silicon Valley Chapter & SEMI International
Symposium Co-Sponsored by IEEE EPS, EDS, Photonics Societies; SEMI Int'l; ASME EPPD

REGISTRATION TYPE (fee includes refreshment breaks and lunches)	**Close of Registration**	**FEE**
1. **HIR Sponsor/Organizing Committee** – fee waived For designated and invited attendees from ASME, IEEE-EDS, IEEE-EPS, IEEE-Photonics and SEMI. Please enter organization name and your name when prompted, or enter assigned code.	20 Feb 2019	Waived
2. HIR Technical Working Group (TWG) Member For contributing and invited members of HIR TWGs. Please register here if you are attending event in person, or enter assigned code.	20 Feb 2019	Waived
3. Corporate Exhibitor & Sponsor For Corporate sponsor: tabletop and banner display space provided; fee waived for up to 5 employees of the corporate sponsor.	20 Feb 2019	$1,000.00
4. General admission and non-member ($10 more after Feb 8)	21 Feb 2019	$40.00
5. IEEE/ASME member; Employee of SEMI member company ($10 more after Feb 8) *This fee applies also to students, retired, unemployed*	21 Feb 2019	$25.00

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Plenary Speaker

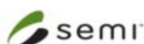
BABAK SABI

Babak Sabi is a corporate vice president and general manager of the Assembly Test Technology Development. Since 2009, he has been responsible for the company's packaging, assembly process, packaging materials, enabling technology, and test technology development. Sabi joined Intel in 1984.

Prior to leading ATTD, Sabi led the Corporate Quality Network within Intel's Technology and Manufacturing Group from 2002 to 2009. He led a company-wide network of quality and reliability organizations responsible for product reliability, customer satisfaction and quality business practices.

Previously, Sabi managed technology development quality and reliability, and was responsible for silicon technology certification, assembly, test and board processes.

Sabi received his Ph.D. in solid state electronics from The Ohio State University in 1984. He has written 10 papers on reliability physics and has received five Intel Achievement Awards. He currently holds two patents.



MAP

Some Hotels Nearby

List Hotel near SEMI Milpitas

<u>Tips for travelling to Silicon Valley.</u>

1. Book your hotels early as rooms usually fill up on weekdays.
2. Road Congestion times: 7:00-10:00 AM & 2:30-7:30 PM
3. Lyft and Uber are very convenient to get around in Silicon Valley
4. Fly into San Jose Airport, California (SJC); 20 minutes to SEMI venue

   Not to be confused with San Jose Airport, Costa Rica (SJO)

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