IEEE
Heterogeneous Integration Roadmap (HIR) Symposium

2nd Annual, intro to HIR v1.0, overviews, integration, working groups, participation …
HIR v1.0 Roadmap Release

Co-hosted by IEEE-EPS Santa Clara Valley Chapter & SEMI

When: February 21 - 22, 2019
Where: SEMI Headquarters, 673 South Milpitas Blvd, Milpitas, CA
Cost: $25 IEEE/ASME members, students, unemployed; $40 non-members. ($10 more after Feb. 10th) (includes lunch)
Registration waived for HIR Technical Working Group (TWG) members

Register Now: **http://www.cpmt.org/scv/?p=818**

Note: photographs and videos will not be permitted during the Symposium

Thursday, February 21, 2019: HIR Symposium *(details below)*
Time: 8:30 AM – 6:00 PM
Who Should Attend: Open to the General Public
Speakers: Chairs of Working Groups (from Intel, Boeing, Fraunhofer, NASA, Infineon, Google, Advantest, StatsChipPaC, Dow, ASE, ITRI, SEMI, more)

Friday, February 22, 2019: HIR Technical Working Meeting and Open House
Time: 8:30 AM – 4:00 PM
Who Should Attend: All HIR Technical Working Group members and anyone interested in participating or learning more about and participating in the Heterogeneous Integration Roadmap.
The purpose is to provide a forum for interaction, collaboration and feedback.

Information and registration: **http://www.cpmt.org/scv/?p=818**

Summary: *Heterogeneous Integration* will be the key technology direction going forward, for device and subsystem integration. It is the "low hanging fruit" for initiating a new era of technological and scientific advances to continue and complement the progression of Moore's Law scaling into the distant future. Presentations from HIR Technical Working Group chairs. Corporate sponsorships/exhibits available. The agenda for Roadmap Symposium follows:

IEEE HIR ROADMAP MORNING Program Thursday Feb 21, 2019

8:30 – 9:00 am	**REGISTRATION & COFFEE**
9:00 – 9:15 am	**SYMPOSIUM OPENING: William Chen** (HIR)
	Welcome : Ajit Manocha, President & CEO SEMI
	Nicky Lu, CTO and Chairman, Etron Technology Inc.

Session 1 Chair: Bill Bottoms 3MTS
9:15 – 10:50am **Heterogeneous Integration for High Performance**

- High Performance Computing & Data Center: Kanad Ghose (Binghamton University), Dale Becker (IBM)
- 3D & Interconnect: Ravi Mahajan (Intel)

- WLP (fan in and fan out): Rozalia Beica (DOW), John Hunt (ASE)
- Thermal Management: Madhu Iyenger (Google), Azmat Malik (Acuventures)
- Integrated Photonics: Amr Helmy (University of Toronto), Bill Bottoms (3MTS)
- Test: Dave Armstrong (Advantest)

10:33 -10:50am Q&A
BREAK

Session 2 Chair: Ravi Mahajan, Intel
11:05 – 12:40pm **Heterogeneous Integration for Consumer & Industrial Applications**

- Emerging Devices: Meyya Meyyappan (NASA Ames)
- Medical and Health & Wearables: Mark Poliks (Binghamton U), Nancy Stoffel (GE)
- SiP & Module: Rolf Aschenbrenner (Fraunhofer IZM), Klaus Pressel (Infineon)
- Single Chip and Multi Chip Integration: William Chen (ASE), Annette Teng (Promex)
- Integrated Power Package: Patrick McCluskey (UMD), Doug Hopkins (NCSU)
- IoT: Robert Lo (ITRI Taiwan)
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12:23 – 12:40pm Q&A
12:40 – 1:40pm **LUNCH**
1:40 – 2:25pm **PLENARY PRESENTATION**
Invited Speaker: Babak Sabi, Corporate Vice President, General Manager of Assembly & Test Development, Intel Corporation

Session 3 Chair: Tom Salmon, SEMI
2:25 – 3:45pm **Heterogeneous Integration for Special Applications**

- Aerospace & Defense: Tim Lee (Boeing)
- 5G in RF and Analog Mixed Signal: Tim Lee (Boeing), Herbert Bennett (Alta Tech)
- Cyber Security: Sohrab Aftabjahani (Intel)
- Simulation: Chris Bailey (University of Greenwich), Xuejun Fan (Lamar University)
- MEMS & Sensor Integration: Shafi Saiyed (ADI)

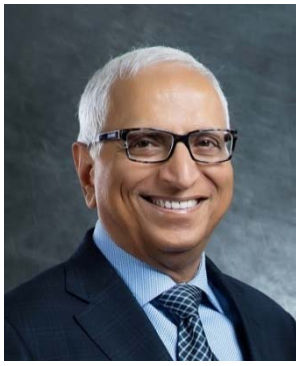
3:25-3:45pm Q&A
BREAK

Session 4 Chair: Amr Helmy, Univ of Toronto
4:00 – 5:15pm **Heterogeneous Integration Applications, Materials & Simulation**

- Automotive: Urmi Ray (STATS ChipPAC), Rich Rice (ASE)
- Mobile: William Chen (ASE)
- Materials & Emerging Research Materials: Bill Bottoms (3MTS)
- Supply Chain: Tom Salmon (SEMI)

4:48 – 5:15pm Q&A
5:15 – 5:30pm Information on Release of HIR version 1.0: Download & Roadmap Use
5:30 pm **WRAP UP: Nicky Lu, CTO and Chairman, Etron Technology Inc.**
SYMPOSIUM CLOSING

Babak Sabi is a corporate vice president and general manager of the Assembly Test Technology Development. Since 2009, he has been responsible for the company's packaging, assembly process, packaging materials, enabling technology, and test technology development. Sabi joined Intel in 1984.
Prior to leading ATTD, Sabi led the Corporate Quality Network within Intel's Technology and Manufacturing Group from 2002 to 2009. He led a company-wide network of quality and reliability organizations responsible for product reliability, customer satisfaction and quality business practices.
Previously, Sabi managed technology development quality and reliability, and was responsible for silicon technology certification, assembly, test and board processes.



Sabi received his Ph.D. in solid state electronics from The Ohio State University in 1984. He has written 10 papers on reliability physics and has received five Intel Achievement Awards. He currently holds two patents.

Ajit Manocha is the president and CEO of SEMI. Headquartered in Milpitas, California, SEMI is the global industry association serving the electronics manufacturing supply chain. Manocha, an industry leader has over 35 years of global experience in the semiconductor industry.

Manocha was formerly CEO at GLOBALFOUNDRIES, during which he also served as vice chairman and chairman of the Semiconductor Industry Association (SIA). Earlier, Manocha served as EVP of worldwide operations at Spansion. Prior to Spansion, Manocha was EVP and chief manufacturing officer at Philips/NXP Semiconductors. He began his career at AT&T Bell Laboratories as a research scientist where he was granted several patents related to microelectronics manufacturing.

Today, there is a much broader scope for SEMI to help foster collaboration and fuel growth than we could have ever imagined at SEMI's inception in 1970. This has to be accomplished without compromising the strong foundation of SEMI comprising of Equipment Suppliers and Materials makers. Given our ecosystem is rapidly expanding due to the massive explosion of applications based on the Internet and mobile devices, biomedical devices, defense, social media, artificial intelligence/machine learning, autonomous vehicles e-commerce, the Internet of Things, etc., Manocha feels it is the right time for us to evolve as the space around us evolves.

Additionally, Manocha has served on the President's committees for "Advanced Manufacturing Partnerships" and the President's Council of Advisors on Science & Technology (PCAST) during the last 4+ years.

Dr. Nicky Lu is the Chairman, CEO & Founder, Etron Technology, Inc. and Managing Board Director, Taiwan Semiconductor Industry Association (TSIA). As a researcher, design architect, entrepreneur and chief executive, Dr. Lu has dedicated his career to the worldwide IC design and semiconductor industry. He also co-founded several other high-tech companies including Ardentec, Global Unichip and GTBF Corporations.

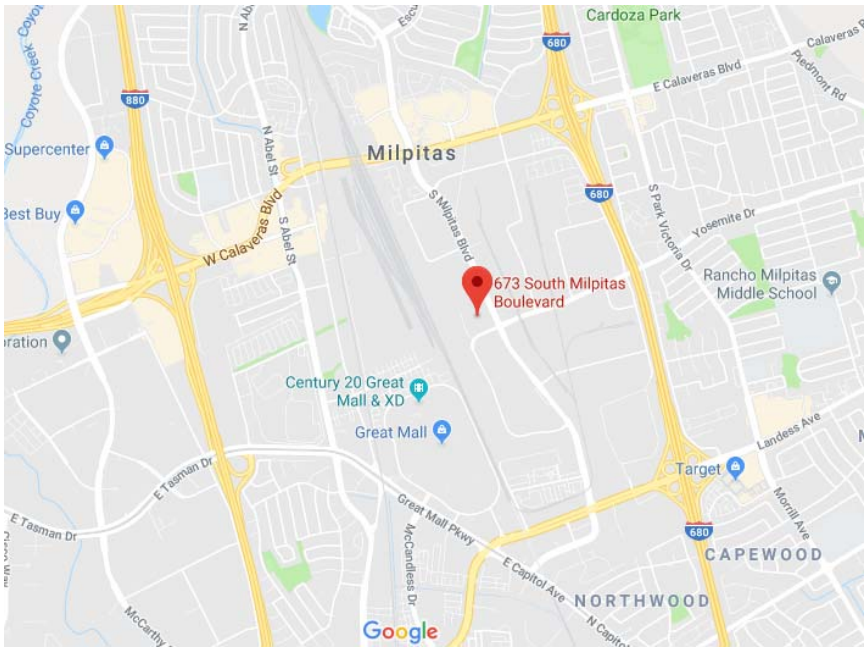
Dr. Lu worked for the IBM Research Division and then the Headquarters from 1982 to 1990 and won numerous IBM recognition awards, including an IBM Corporate Award. He co-invented and pioneered a 3D-DRAM technology, known as the Substrate-Plate Trench-Capacitor (SPT) cell, along with its associated array architecture, which has been widely used by IBM and its licensees from 4Mb to 1Gb DRAMs and embedded DRAMs over hundreds of billions dollars. Dr. Lu designed several High-Speed CMOS DRAM (HSDRAM) chips, with all top worlds' records of performance. He was a co-architect leading the 8-inch wafer and DRAM/SRAM/LOGIC technology developments for Taiwan semiconductor industry in early 1990s, also created many Taiwan companies as prominent silicon-chip suppliers. Since 1999 he has pioneered Known-Good-Die Memory Products enabling 3D stacked-dices system chips; this work summoned the new rise of an IC Heterogeneous Integration Era as described in his ISSCC-2004 plenary talk, demonstrating a new 3D-IC trend. He was a keynote speaker at the 2016 A-SSCC disclosing Silicon-Age-4.0 Era with a new Virtual Moore's Law as a indicator of continual economic growth.

Dr. Lu received his B.S. in Electrical Engineering from National Taiwan University and M.S. and Ph.D. in EE from Stanford University. He holds over 30 U.S. patents and has published more than 60 technical papers. He serves as Managing Board Director and was Chairman of TSIA, as Board Member of Global Semiconductor Alliance (GSA) and GSA's General Chair (2009 to 2011), and Chairman of WSC (World Semiconductor Council) from 2014 to 2015.

He received the Scientific Management Award (2012) from Chinese Society for Management of Technology and Taiwan's Golden Merchant Award (2007) from General Chamber of Commerce. He is an Outstanding Alumnus of National Taiwan University, a Chair Professor and an Outstanding Alumnus of National Chiao Tung University, an IEEE Fellow, the recipient of the IEEE 1998 Solid-States Circuits

Award, a member of NAE (National Academy of Engineering of USA), and received of a SEMI Industry Contribution Award in 2017.

Map of SEMI HQ Surroundings



Nearby Hotels (within approx. 10-minute drive)

- Embassy Suites
- Hilton Garden Inn San Jose/Milpitas
- Crown Plaza San Jose-Silicon Valley
- Extended Stay America San Jose - Milpitas McCarthy Ranch
- Best Western Plus Brookside Inn
- Residence Inn by Marriott Milpitas Silicon Valley
- Baymont by Wyndham Milpitas/San Jose